UNIVERSITY OF NOVA GORICA GRADUATE SCHOOL

Nanoscale electric charge transport in organic thin film transistors

Dissertation

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Nova Gorica, 2009

Acknowledgments

Several people helped me in the experimental work and in the theoretical analysis of the data presented in this thesis. First, I would like to thank my advisor prof. dr. Gvido Bratina for all the help during my Ph.D. research and in writing this thesis. I would like to extend my thanks to my colleagues dr. Egon Pavlica, Primož Rebernik Ribič, mag. Peter Krkoč, Alan Batagelj and dr. Polona Skraba for productive discussions which helped me in understanding of numerous details about my work and fruitful suggestion regarding the setup and realisation of my experiment. This work would not be possible without the help of prof. dr. Lucia Sorba and two former members of AMD group dr. Daniele Ercolani and Tomaž Mlakar from TASC National Laboratory, Trieste, Italy and prof. dr. Enzo Di Fabrizio, dr. Massimo Tormen, Alessandro Carpentiero and former member of LILIT dr. Marco Matteucci from Elettra Synchrotron, Trieste, Italy, who helped me with the optical and electron-beam lithography. Special thanks goes to my parents and my girlfriend Ana who supported me during my years of studying and understood my moods connected with successes and failures in my work.

Π

Abstract

We have investigated charge transport properties in pentacene-based organic thin film transistors (OTFTs). The characterisation of OTFTs was performed in situ, during evaporation of pentacene active layers, and after the pentacene layers were deposited, and ex situ, by atomic force microscopy (AFM) and by Kelvin force microscopy (KFM).

In the first part, our work was focused on the fabrication and optimisation of the source-drain metallic. Source and drain metallic contacts were fabricated by single layer optical lithography, double layer optical lithography, electron-beam lithography and by thermal evaporation of Ti and Au. Samples with different Ti layer thickness were fabricated. The contacts comprised 2 nm to 3 nm-thick Ti layer, covered by 30 nm to 50 nm-thick Au layer. Control samples without Ti adhesion layer were also fabricated. The electrical characterisation of OTFTs was performed in situ by following the evolution of source-drain current during the deposition of pentacene layers. Morphological evolution of pentacene layers for the increasing coverages were investigated ex situ by AFM. Electrical investigation showed that the influence of Ti adhesion layer used in the source-drain contact fabrication process, can influence the charge transport properties of OTFTs. In addition, based on the morphological observation of pentacene layers, and the evolution of source-drain current, we concluded that the majority of mobile charge, and therefore, the thickness of transport layer is limited inside the first-two monolayers of pentacene.

In the second part of our work we investigated the influence of the SiO_2 surface treatment and the deposition conditions on the contact resistance at the Au/pentacene interfaces. The origin of the contact resistance is ascribed to the morphological defects in the semiconductor layer in the vicinity of the source-drain electrical contacts and to the hole injection barrier at the Au/pentacene interface. Our morphological investigation by AFM showed that the surface treatment of SiO_2 by hexamethyldisilazane (HMDS) promotes adhesion between Au and pentacene and improves the morphology of pentacene layers near the Au contacts. The influence of deposition conditions was investigated by monitoring the source-drain current during the evaporation of pentacene layers as a function of layer thickness. Our results showed that the effective field-effect mobility of OTFTs decreased with the decreasing growth rates. We associated the decrease in mobility for the low growth rates (< 0.05 nm/min) and for the high substrate temperatures $(\sim 80^{\circ}\text{C})$ to a high degree of the structural defects at the Au/pentacene interface. Less obvious morphology/mobility correlation was observed for the growth rates ranging between 0.15 nm/min and 2 nm/min and for the substrate temperatures ranging between 25°C and 65°C, therefore, additional electrical characterisation was performed ex situ by KFM. Results showed that the contact resistance at the Au/pentacene interfaces is the critical factor for optimum transistor operation. We showed that the contact resistance can be optimised by tuning the deposition parameters.

In the last part of our work we investigated the influence of the pentacenebased OTFTs exposure to ambient air. Time-depended electric charge transport measurements of OTFTs were coupled to Kelvin force probe microscopy, demonstrating that exposure of OTFTs to ambient air for extended periods of time, results in two competitive mechanisms that were responsible for the observed variation in the source-drain current. Relatively fast oxygen doping through electronegativity-related creation of holes increases the carrier concentration. This results in a lower energy barrier at the Au/pentacene interface, promoting thereby charge injection from the metal contact into the pentacene layer. Slower, and persistent mechanism of water diffusion in the pentacene layer induces dipole-charge carrier interactions through the creation of energetic disorder. This results in long-term reduction of the source-drain current. KFM measurements allowed us to follow the evolution of resistance in time at the source/pentacene, the drain/pentacene and inside the channel, separately. Consequently, we were able to determine which part of OTFTs was more sensitive and thus responsible for the degradation in charge transport after the prolonged exposure to ambient air.

Keywords

organic semiconductors, organic thin film transistors, microlithography, organic molecular beam deposition, atomic force microscopy, Kelvin force probe microscopy, contact resistance

TRANSPORT NABOJA V ORGANSKIH TANKOSLOJNIH TRANZISTORJIH

I. Uvod

Do prvih raziskav na področju organskih polprevodnikih (OP) je prišlo že v poznih 40-ih letih prejšnjega stoletja [1]. Glavne prednosti aplikacij narejenih iz OP so: nizka produkcijska cena, ki je posledica nizkotemperaturnih procesov povezanih z nanosom aktivnih plasti OP; primerne mehanske lastnosti OP, ki dovoljujejo proizvodnjo gibljivih naprav in možnost nanašanja OP plasti na razsežnih površinah.

Velik premik v raziskavah OP se je zgodil sredi 80-ih let, s produkcijo prve nizkovoltne organske LED svetilke [2]. Razvoj se je nadaljeval z izdelavo tankoslojnega organskega tranzistorja (OTT) z aktivno plastjo pentacena, ki je dosegel mobilnost nosilcev naboja $\mu \sim 1 \text{ cm}^2/\text{Vs}$, kar je primerljivo z mobilnostjo naboja v amorfnem silicijevem kristalu [1].

Vrednost mobilnosti nosilcev naboja v OP je najpomembnejši parameter, ki določa potencialno uporabnost določenega OP, zato so se razvile številne metode, s katerimi lahko merimo vrednost mobilnosti [4]. Pri naših raziskavah smo za merjenje mobilnosti nosilcev naboja uporabili metodo, ki temelji na meritvah toka skozi OTT. Pri tem je bilo treba upoštevati, da na tok skozi OTT vplivajo tudi drugi parametri kot so: upor na izvirni in ponorni elektrodi; morfologija OP plasti; obdelava plasti izolatorja s snovmi, ki spremenijo omočljivost površine izolatorja in izpostavljenost OP atmosferskemu zraku.

Upor na meji med izvirno elektrodo in OP se povezuje predvsem z energijsko bariero za injekcijo nosilcev naboja, ki je posledica zamika med Fermijevo energijo kovinskega kontakta in vrhom valenčnega pasu (highest occupied molecular orbital - HOMO) v OP [8]. Upor pa se pojavi tudi zaradi strukturnih nepravilnosti v plasti OP na meji obeh elektrod [49]. Eden od načinov, s katerim lahko merimo upor na meji med OP in elektrodami, je metoda Kelvinove mikroskopije (KM).

Tudi morfologija (velikost otokov) v plasteh OP lahko vplivala na delovanje OTT. Ker je transport naboja po OP odvisen od prekrivanja molekulskih orbital, predstavljajo stiki na meji med otoki oviro za transport naboja [9]. Velikost otokov lahko kontroliramo s hitrostjo naparevanja OP in temperaturo substrata, na katerega OP naparevamo [10]. Dodatno lahko vplivamo na morfologijo OP z obdelavo izolatorja, na katerega OP nanašamo, s snovmi, ki spremenijo omočljivost površine izolatorja.

Na električno in morfološko stabilnost OP vpliva izpostavljenost atmosferskemu zraku - difuzija predvsem kisika in vodne pare v plasti OP. Vpliv atmosferskega zraka na delovanje OTT je pomemben tako iz vidika stabilnosti OTT na zraku, kot tudi iz vidika optimizacije plinskih senzorjev, ki imajo aktivno plast narejeno iz OP.

II. Lastnosti organskih polprevodnikov

Za transport naboja po OP je pomembno prekrivanje med π orbitalami sosednjih molekul. Na intenzivnost prekrivanja vplivata morfologija in kristalna struktura, na oboje pa lahko vplivamo z metodo in parametri nanosa OP plasti. Metoda nanosa je odvisna predvsem od fizikalnih in kemičnih lastnosti določenega OP [3]. Za OP, ki so netopni v organskih topilih, se za nanos uporablja metoda vakuumskega naparevanja, medtem ko se za OP, ki so topni v organskih topilih, uporabljajo različne kapljične metode nanašanja.

OP so zgrajeni iz električno nevtralnih molekul. Osnovni gradniki molekul, ki tvorijo OP, so benzenovi obroči. p_z orbitale, ki pripadajo posameznemu atomu ogljika, so pravokotne na ravnino benzena (Slika 2.2 (a)). Ker je razdalja med atomi ogljika dovolj majhna, pride do prekrivanja p_z orbital in do tvorbe π vezi. Elektroni, ki sodelujejo v π vezi, so relativno šibko vezani na določen ogljikov atom. V benzenovem obroču zato nad in pod ravnino benzena nastanejo delokalizirani oblaki elektronov [17]. Zaradi delokalizacije elektronskih orbital lahko pride do interakcije in posledično do transporta naboja med sosednjimi molekulami. Pozitivni naboj v OP potuje po vrhu valenčnega pasu (HOMO), negativni naboj pa po dnu prevodnega pasu (lowest unoccupied molecular orbital - LUMO) [18].

V naših OTT smo za aktivno plast OP uporabili pentacen. To je polarna molekula, dolga 1.5 nm, ki jo sestavlja 5 benzenovih obročev (Slika 2.1 (a)) [19]. Pentacen je polprevodnik p-tipa. Energijska špranja med HOMO in LUMO je 2.6 eV [20]. Ima triklinsko kristalno strukturo. Molekule so v plasti urejene v srtast vzorec (herringbone). Ureditev je posledica interakcije med delokaliziranimi π orbitalami, ki preferirajo čelno prekrivanje pentacenovih molekul in kvadrupolne interakcije, ki preferira orientacijo roba in ploskve pentacenovih molekul (Slika 2.3 (b)) [15,21]. Intenzivnost prekrivanja molekulskih orbital lahko ocenimo iz razdalj med molekulami in iz njihove orientacije. Pokaže se, da je prekrivanje molekulskih orbital med molekulami v ravnini veliko večje kot med molekulami, ki so pravokotne na ravnino. To posledično privede do izotropnega transporta naboja po plasteh pentacena [21].

Za plasti pentacena, ki so pripravljene z metodo vakuumskega naparevanja, sta znani dve kristalni fazi. Med seboj se razlikujeta po debelini posameznih slojev. Meritve so pokazale, da je za transport naboja primernejša tankoslojna faza (thin-film phase), saj pride na mejah med otoki do boljšega prekrivanja molekulskih orbital in s tem do boljšega transporta naboja po plasti pentacena [25].

III. Transport naboja v organskih polprevodnikih

Fizikalni procesi, ki so odgovorni za transport naboja v OP, so bili predmet preučevanja številnih raziskovalnih skupin [4, 16, 18, 26-29]. Modeli, s katerimi opisujemo transport naboja v OP, bazirajo na modelih, ki so bili razviti za opis transporta naboja v anorganskih polprevodnikih. Razlog za zgornjo posplošitev lahko iščemo v dejstvu, da so vplivi (npr. temperature in električnega polja) na gibljivost nosilcev naboja v OP pogosto podobni kot v anorganskih polprevodnikih [27,30-33].

V polprevodnikih ločimo dva ekstremna tipa transporta naboja. Prvi je pasovni tip transporta naboja, kjer nosilce naboja opišemo z delokaliziranimi ravnimi valovi in se pri opisu naslonimo na Blochov formalizem [34]. V drugem primeru so nosilci naboja močno lokalizirani, tako da je transport mogoč le s preskakovanjem naboja med lokaliziranimi stanji [17]. Glavna značilnost pasovnega načina transporta je velika mobilnost naboja $\mu \gg 1$ cm²/Vs in temperaturna odvisnost mobilnosti, ki jo opišemo kot $\mu \propto T^{-1}$, n > 1. V drugem primeru pa je vrednost mobilnosti $\mu < 1$ cm²/Vs in z nižanjem temperature pada [26, 35].

V OP opazimo oba tipa transporta. V neurejenih OP (npr. v konjugiranih polimerih) opišemo transport nosilcev naboja s preskakovanjem naboja med lokaliziranimi stanji [16, 30, 31, 36, 37]. Ker k preskakovanju pripomore udeležba fononov, se mobilnost naboja poveča z višanjem temperature, a kljub temu ostane relativno nizka ($\mu < 1 \text{ cm}^2/\text{Vs}$). Nasprotno lahko pri urejenih organskih monokristalih, ki so sestavljeni iz majhnih oligomernih molekul (npr. naftalen), opazimo pasovni tip transporta, pri katerem se mobilnost veča z nižanjem temperature in doseže vrednost $\mu \sim 400 \text{ cm}^2/\text{Vs}$ pri T = 4.2 K [33, 38].

IV. Organski tankoslojni tranzistorji

Tranzistorji z vplivom polja (field-effect transistors) so elektronske na-

prave, pri katerih z električnim poljem kontroliramo velikost toka skozi kanal v aktivni plasti polprevodnika. Če je aktivna plast narejena iz organskega polprevodnika, tako napravo imenujemo organski tranzistor z vplivom polja. Najpogostejša konfiguracija organskega tranzistorja z vplivom polja je organski tankoslojni tranzistor.

Najpogosteje uporabljeni geometriji za izdelavo OTT sta predstavljeni na Sliki 4.1. Pri bottom-contact, bottom-gate (BB) geometriji izolator ločuje vrata (gate) od plasti OP ter izvirnih in ponornih elektrod (source, drain electrodes), ki so izdelane pred nanosom OP. Obraten proces je prisoten pri izdelavi OTT z top-contact, bottom-gate (TB) geometrijo. Pri TB geometriji se plast OP nanese pred izdelavo elektrod. Glavna prednost BB geometrije je možnost izdelave izvirnih in ponornih elektrod z zelo majhnim razmikom med elektrodama. Dodatna prednost je možnost postavitve eksperimenta, pri katerem lahko izvedemo električno karakterizacijo OTT vzorcev med nanašanjem aktivne plasti OP ter tako sledimo spremembam toka skozi OTT z debelino aktivne plasti OP [52, 53]. Glavne komponente OTT so torej: vrata, plast izolatorja, izvirne in ponorne elektrode ter aktivna plast OP.

Z napetostjo na vratih kontroliramo gostoto naboja na meji med izolatorjem in plastjo OP. V mnogih primerih se vrata uporabljajo tudi kot substrat, na katerega je nanešen izolator. V OTT so vrata najpogosteje narejena iz Si rezine s primesjo [1, 3].

Plast izolatorja preprečuje tok med vrati in OP ter izvirno in ponorno elektrodo. Glavne karakteristike izolatorjev, ki so primerni za OTT, so: velika dielektrična konstanta, visoka prebojna napetost in nizka površinska hrapavost. Vse potrebne karakteristike združuje SiO_2 , zato je kljub številnim organskim in anorganskim dielektrikom, ki so na voljo, najpogosteje uporabljen v OTT [56].

Funkcija izvirne elektrode je injekcija električnega naboja v aktivno plast OP, funkcija ponorne elektrode pa črpanje električnega naboja iz OP. Najpogosteje uporabljen material za pripravo izvirnih in ponornih elektrod v OTT je Au.

Princip delovanja tankoslojnega tranzistorja je prikazan na Sliki 4.2 [27]. Napetost na OTT se pripelje na vrata (V_g) in na ponorno elektrodo (V_d) , medtem ko je izvirna elektroda ozemljena $(V_s = 0 \text{ V})$. Razliko med električnim potencialom na izvirni in ponorni elektrodi označimo z V_{sd} . Ko priključimo negativno napetost na vrata, pride na stiku med izolatorjem in plastjo OP do akumulacije pozitivnega naboja. Gostota induciranega naboja je odvisna od napetosti V_g in kapacitete izolatorja. Ves naboj pa ni gibljiv, saj se ga del ujame zaradi prisotnosti električno-aktivnih pasti, ki so posledica strukturnih in kemičnih nepravilnosti na stiku med izolatorjem in plastjo OP. Tok

VIII

skozi OTT opazimo šele, ko na vrata pripeljemo dovolj veliko negativno napetost, ki ji pravimo pragovna napetost (V_{th}) . Zaradi prisotnosti pasti se torej napetost V_q zmanjša na efektivno napetost $(V_q - V_{th})$.

Na sliki 4.2 (b) je predstavljeno stanje, ko ponorno elektrodo ozemljimo in pripeljemo negativno napetost na vrata ($V_s = V_d = 0$ V; $V_g < 0$ V). V tem primeru pride do akumulacije pozitivnega naboja, ki je enakomerno porazdeljen čez celoten kanal OTT. Tok skozi OTT opazimo, ko pripeljemo majhno negativno napetost na ponorno elektrodo (($V_d < 0$ V; $|V_g| > |V_{th}|$). S poviševanjem napetosti V_d v negativni smeri, linearno povečujemo tok skozi OTT. Dokler velja linearna odvisnost med tokom in napetostjo V_d , OTT deluje v linearnem načinu. Taka odvisnost velja vse do $V_d \sim V_g - V_{th}$ (Slika 4.2 (c)), ko se ob ponorni elektrodi ustvari območje brez gibljivega naboja. Od tu naprej se z višanjem napetosti V_d tok skozi OTT ne povečuje več. Pravimo, da tranzistor deluje v nasičenju (Slika 4.2 (d)).

V. Eksperimentalne metode

Naparevanje organskega materiala

V našem eksperimentu smo za aktivno plast v OTT uporabljali pentacen. Kot že rečeno, pentacen ni topem v organskih topilih, zato smo za pripravo aktivnih plasti v OTT uporabljali metodo vakuumskega naparevanja. Naparevanje je potekalo v vakuumski komori (Slika 5.3) pri tlakih, ki so bil običajno nižji od 10^{-5} Pa. Potekalo je tako, da smo pentacen, ki se je nahajal v izparilnih celicah, segreli do izparilne temperature. S kontoliranjem temperature na izparilnih celicah smo lahko določali hitrost naparevanja. Pri pentacenu je bila temperatura v izparilnih celicah med 120°C in 170°C. Curke molekul smo usmerili proti substratom, na katerih smo želeli vzgojiti aktivne plasti. Temperaturo na substratih smo uravnavali s pomočjo grelca, ki je bil pritrjen na nosilec za vzorce (Slika 5.4), in se je gibala med 20°C in 80°C. Glavni prednosti nanašanja materiala z metodo vakuumskega naparevanja sta visoka čistost in nanometerska kontrola nad debelino plasti.

Električna karakterizacija OTT

V tem podpoglavju je opisana električna karakterizacija OTT, ki smo jo izvedli po naparevanju aktivne plati pentacena. Električna karakterizacija je običajno potekala v vakuumu z merjenjem toka skozi OTT. S pomočjo tovrstnih meritev smo lahko določili vrednosti mobilnosti, pragovne napetosti ter vrednosti razmerja med tokom zaprtega in odprtega tranzistorja.

I - V karakterizacija je potekala tako, da smo merili tok skozi OTT pri

konstantni vrednosti V_g in s spreminjanjem V_d . Meritve smo ponovili za različne vrednosti V_g . Krivulje toka v odvisnosti od V_d za različne V_g so prikazane na Sliki 5.5 in so nam omogočile izračun mobilnosti. Merjenje transkonduktance je potekalo tako, da smo merili tok skozi OTT pri konstantni vrednosti V_d in s spreminjanjem V_g . Krivulji toka v odvisnosti od V_g za različni vrednosti V_d sta prikazani na Sliki 5.6 (a) in Sliki 5.6 (b). Z merjenjem transkonduktance pri majhnih vrednostih V_d smo izračunali vrednost pragovne napetosti, z merjenjem transkonduktance pri velikih vrednostih V_d pa smo izračunali vrednost razmerja med tokom zaprtega in odprtega tranzistorja.

Električne meritve so pokazale velike razlike med vrednostmi mobilnosti, pragovne napetosti in razmerja med tokom zaprtega in odprtega tranzistorja. Vrednost mobilnosti je nihala med 10^{-4} cm²/Vs in 0.25 cm²/Vs. Razlike v mobilnosti med vzorci smo pripisali različnim pogojem naparevanja pentacena (hitrost naparevanja in temperatura substrata) in uporabi različnih metod za pripravo električnih kontaktov. Tudi vrednost pragovne napetosti se je med vzorci spreminjala in je nihala med -15 V in +5 V. Nihanje pragovne napetosti se povezuje z vplivom različne gostote električnih pasti na meji med izolatorjem in polprevodnikom ter na meji med otoki v plasti polprevodnika [95]. Vrednost razmerja med tokom zaprtega in odprtega tranzistorja je nihala med 10^3 in 10^5 . Tok skozi OTT v zaprtem stanju se je povečeval zaradi puščanja tranzistorjev skozi izolator (razmerje se je zmanjševalo) in tok skozi OTT v odprtem stanju se je povečeval z optimizacijo OTT, saj je pri dobro delujočih tranzistorjih tekel velik tok v odprtem stanju tranzistorja (razmerje se je povečevalo).

Mikroskopiranje z mikroskopom na atomsko silo

Po nanosu pentacena je sledila morfološka in dodatna električna karakterizacija organskih plasti z mikroskopom na atomsko silo (MAS). Osnovni princip delovanja MAS je merjenje sil med ostro konico pripeto na vzvod in površino substrata, zaradi katerih pride do ukrivljanja oz. dinamičnih sprememb vzvoda, ki jih lahko merimo in signale prevedemo v opazovane količine (morfologija površine, porazdelitev naboja po površini itd.).

Pri našem delu smo s pomočjo MAS raziskovali morfološke (velikosti otokov, morfološke nepravilnosti na stiku med plastjo pentacena in kovinsko elektrodo itd.) in električne lastnosti (padce napetosti na stikih med izvirno elektrodo in pentacenom ter ponorno elektrodo in pentacenom) plasti pentacena. Morfologijo plasti smo opazovali z MAS, ki je deloval v nekontaktnem načinu, pri katerem je nihajoča konica pripeta na vzvod oddaljena od vzorca med 1 nm in 10 nm. Na teh razdaljah pričnejo med konico in vzorcem delovati privlačne van der Waalsove sile, ki povzročijo premik v lastni frekvenci vzvoda. Prek merjenja amplitud vzvoda in popravkov le-teh, lahko računalnik rekonstruira morfološko sliko površine vzorca. Padce napetosti med električnimi kontakti in plastjo pentacena smo merili s pomočjo Kelvinove mikroskopije. Meritev je potekala tako, da smo na konico pripeljali dodaten nihajoč napetostni signal, ki je omogočil elektrostatično interakcijo med površino in konico. Z merjenjem napetosti, ki je bila potrebna, da smo zadušili nihanje vzvoda zaradi dodatnega izmeničnega napetostnega signala, smo lahko merili potencial na površini.

Obdelava površine izolatorja

Obdelava površine izolatorja je bil pomemben korak pri pripravi vzorcev (izdelava izvirnih in ponornih elektrod) in pri optimizaciji OTT (obdelava površine s heksametildisilazanom (HMDS)). Vpliv posameznih snovi in postopkov na površino SiO₂ smo določili s pomočjo meritev kontaktnega kota med vodno kapljico in površino SiO₂ (Slika 5.9 in Slika 5.10).

Pri pripravi vzorcev je bilo treba površino SiO_2 obdelati z NH₃ in O_2 plazmo. V obeh primerih so meritve pokazale, da se omočljivost SiO_2 po obdelavi poveča. Drugačen rezultat smo dobili, ko smo SiO_2 prekrili z eno plastjo heksametildisilazana (HMDS). Meritve kontaktnega kota so pokazale, da se omočljivost SiO_2 po obdelavi zmanjša. Vpliv HMDS na delovanje OTT je predstavljen v poglavju VIII.

VI. Priprava izvirnih in ponornih elektrod

Izvirne in ponorne elektrode smo pripravili z optično in elektronsko litografijo. Optična litografija je metoda, ki za jedkanje uporablja UV svetlobo z valovno dolžino med 300 nm in 450 nm. Mejna velikost vzorcev na substratu, ki jih lahko naredimo z optično litografijo, je ~ 1 μ m. Pri elektronski litografiji je orodje za jedkanje curek elektronov. Mejna velikost vzorcev narejenih z elektronsko litografijo je ~ 100 nm [87]. Prednosti optične pred elektronsko litografijo sta predvsem enostavna oprema in hitrost postopka izdelave vzorcev. Prednost elektronske litografije pa je v natančnosti izdelave elektrod.

Glavni koraki potrebni za izdelavo elektrod z optično litografijo so prikazani na Sliki 6.1. Postopek se prične s čiščenjem in obdelavo površine SiO_2 z acetonom, alkoholom in amoniakom. Sledi nanos optično aktivne snovi z metodo kapljičnega nanosa. Naslednji korak je ekspozicija optično aktivne snovi z UV svetlobo skozi masko, ki določa obliko elektrod. Plast optično aktivne snovi, ki jo UV svetloba doseže, postane topna v razvijalcu, v katerega pomočimo vzorec. Postopku razvijanja sledi naparevanje elektrod v vakuumski komori. Odvečni del kovine na vzorcu se odstrani z odstranjevalcem ali acetonom. Postopek priprave elektrod se zaključi z mehanskim odstranjevanjem odvečne kovine z robov elektrod.

Podoben postopek priprave elektrod srečamo tudi pri elektronski litografiji. Ta se od optične loči v kemični sestavi aktivne snovi, ki mora biti občutljiva na curke elektronov. Drugačen je tudi način obsevanja aktivne snovi, saj pri obsevanju ne uporabljamo maske, pač pa obliko elektrod določimo s krmiljenjem tankega curka elektronov po površini aktivne snovi.

VII. Merjenje toka skozi tranzistor kot funkcija debeline organskega polprevodnika: vpliv adhezijske plasti Ti

Priprava in optimizacija elektrod (izvirnih in ponornih) je bila prva naloga, s katero smo se soočili pri preučevanju OTT. Že zelo zgodaj smo ugotovili, da lahko sama priprava elektrod pomembno vpliva na delovanje OTT in da je razloge za različno delovanje OTT treba iskati v vplivu adhezijske plasti Ti na injekcijo električnega naboja v plast pentacena.

Električni kontakti v naših OTT so bili narejeni z metodama optične in elektronske litografije. Sestavljeni so bili iz 2 nm do 3 nm debele adhezijske plasti Ti, na katero je bila nanešena 30 nm do 50 nm debela plast Au. Dodatno smo naredili nekaj kontrolnih vzorcev brez plasti Ti. Električne meritve na zgornjih vzorcih smo izvajali z opazovanjem toka skozi OTT kot funkcijo debeline aktivne plasti pentacena. Tok skozi OTT smo običajno izmerili, ko je prva plast pentacena povezala izvirno in ponorno elektrodo, kar se je zgodilo pri nominalni debelini pentacena 1.5 nm (Slika 7.4). Drugačno obnašanje smo opazili pri vzorcih, ki so bili narejeni s 3 nm debelo plastjo Ti. Pri teh vzorcih smo tok skozi OTT opazili šele pri nominalni debelini pentacena 2.6 nm (Slika 7.4). Opažen zamik v nominalni debelini pentacena, pri kateri je začel teči tok skozi tranzistor, smo povezali z veliko energijsko bariero za injekcijo naboja med Ti in pentacenom [8, 97]. Menimo, da je vpliv debeline adhezijske plasti Ti še toliko bolj pomemben, saj je transport naboja v plasti pentacena skoncentriran v njenem prvem in drugem sloju. Do te ocene smo prišli s primerjavo električnih meritev toka in morfologije različno debelih plasti pentacena.

VIII. Morfologija na stiku elektrod in pentacena: vpliv obdelave površine substrata

Meritve so pokazale, da je morfologija na stiku med OP in elektrodami pomembna za optimalno delovanje OTT [49, 50]. Eden od razlogov za boljše delovanje OTT s TB geometrijo v primerjavi z OTT z BB geometrijo so morfološke nepravilnosti v plasteh OP na stiku z elektrodami, ki nastanejo ob naparevanju OP na že pripravljene elektrode. Zmanjševanje morfoloških nepravilnosti v plasteh OP na stiku z elektrodami je torej ključnega pomena za optimizacijo OTT.

V eksperimentu smo raziskali vpliv hitrosti naparevanja in vpliv obdelave SiO_2 izolatorja na delovanje OTT. V ta namen smo združili rezultate pridobljene z električno karakterizacijo vzorcev med naparevanjem pentacena v vakuumu z rezultati opazovanja morfologije v plasteh pentacena z MAS na zraku.

Pri eksperimentu smo uporabili vzorce, pri katerih so bile izvirne in ponorne elektrode narejene z metodo optične litografije. Razdalje med elektrodami so bile 5 μ m, dolžina elektrod pa 2.3 mm. Elektrode so bile narejene iz 50 nm debele plasti Au. Pod njo je bila naparjena 2 nm debela adhezijska plast Ti.

Vzorce, ki smo uporabili v prvem delu eksperimenta, smo obdelali s HMDS. V tem delu eksperimenta smo merili mobilnost OTT med naparevanjem pentacena pri konstantni temperaturi substrata ($T = 25^{\circ}$ C) in pri treh hitrostih naparevanja: 0.05 nm/min, 0.15 nm/min in 1.2 nm/min. Rezultati so pokazali, da se je mobilnost OTT večala s hitrostjo naparevanja in da je bila oblika krivulj, ki kažejo odvisnost mobilnosti od debeline pentacena, prav tako pogojena s hitrostjo naparevanja (Slika 8.1). Če je bila hitrost naparevanja 0.05 nm/min, se je na krivulji pojavil plato, in sicer pri debelini plasti med 3 nm in 10 nm. Pri preostalih dveh krivuljah se ta plato ni pojavil (Slika 8.1). Nastanek platoja smo pojasnili z opazovanjem morfologije 2 nm, 4.5 nm, 10 nm in 17 nm debelih plasti pentacena (Slika 8.2 in Slika 8.3). Rezultati so pokazali, da je pri nizkih hitrostih naparevanja na stikih nastal kanal, ki je ločeval elektrode od plasti pentacena. Kanal se je pričel polniti šele pri nominalni debelini pentacena 10 nm, kar je posledično privedlo do ponovnega povečevanja toka skoz tranzistor (Slika 8.1).

V drugem delu eksperimenta smo primerjali morfologijo na stiku elektrod in pentacena. Za eksperiment smo pripravili dve vrsti vzorcev: vzorce, pri katerih je bila na površino SiO_2 nanešena plast HMDS in vzorce brez HMDS. Meritve so pokazale, da se z obdelavo SiO_2 površine s HMDS poveča omočljivost med pentacenom in elektrodami (Slika 8.4), kar lahko pripelje do boljšega delovanja OTT.

IX. Upor na elektrodah v organskih tankoslojnih tranzistorjih

Plasti OP naparjene na SiO_2 so sestavljene iz otokov, katerih velikost in oblika je odvisna od pogojev naparevanja, kot sta hitrost naparevanja in temperatura substrata [10]. Raziskave so pokazale, da je mobilnost naboja v plasteh pentacena, ki vsebujejo velike otoke, večja, kot v plasteh, ki jih sestavljajo majhni otoki. Ker je poznavanje korelacije med morfologijo OP in električnimi lastnostmi OTT ključno za optimizacijo OTT, smo tovrstne raziskave izvajali tudi v našem laboratoriju.

V eksperimentu smo raziskali, kako pogoji, pri katerih naparevamo pentacen, vplivajo na upor na posameznih delih OTT, in sicer: na stikih med elektrodami in pentacenom ter v kanalu OTT.

Pri eksperimentu smo uporabili vzorce, pri katerih so bile elektrode narejene s kombinacijo optične in elektronske litografije. Razdalje med elektrodami so bile 4 μ m, dolžina elektrod pa 300 μ m. Elektrode so bile narejene iz 30 nm debele plasti Au. Pod njo je bila naparjena 2 nm debela adhezijska plast Ti. Med seboj smo primerjali tri vrste vzorcev: v skupini I so bili vzorci, na katere smo pentacen naparevali s hitrostjo r = 0.7 nm/min in substrat segreli do temperature $T_{sub} = 80^{\circ}$ C, v skupini II so bili vzorci z r = 0.75 nm/min in $T_{sub} = 50^{\circ}$ C ter v skupini III vzorci z r = 1.6 nm/min in $T_{sub} = 80^{\circ}$ C. Debelina pentacena je bila v vseh primerih 45 nm.

Po nanosu pentacena je sledila električna karakterizacija vzorcev v vakuumu. Najvišjo vrednost mobilnosti smo izmerili za vzorce tipa III, najnižjo pa za vzorce tipa I (Slika 9.1). Električni karakterizaciji v vakuumu sta sledili električna in morfološka karakterizacija na zraku z MAS.

Na Sliki 9.2 (a), ki prikazuje površino vzorca tipa I, vidimo defekte v plasti pentacena. Defekti se pojavijo tako v kanalu tranzistorja kot tudi na stikih med pentacenom in obema elektrodama. Z defekti smo lahko pojasnili najnižjo vrednost mobilnosti, ki smo jo izmerili na vzorcih tipa I. Na Sliki 9.2 (b) je prikazana površina vzorcev tipa II, na Sliki 9.2 (c) pa površina vzorcev tipa III (c). Iz obeh slik vidimo, da nam zgolj morfološka karakterizacija plasti ne more pojasniti vzroka za večjo mobilnost, izmerjeno v vzorcih tipa III v primerjavi z vzorci tipa II, saj sta si morfologiji precej podobni. Za razumevanje električnih meritev iz Slike 9.1 je bilo treba vpeljati metodo KM.

S pomočjo KM smo lahko opazovali padce napetosti na: stiku med izvirno elektrodo in pentacenom, na plasti pentacena v kanalu OTT ter na stiku med pentacenom in ponorno elektrodo. Padce napetosti smo odbrali iz krivulj, ki prikazujejo električni potencial med dvema elektrodama. Primer krivulje za vzorec tipa I je prikazan na Sliki 9.3, vrednosti padcev napetosti pa na Sliki 9.4. Z združitvijo meritev padcev napetosti in meritev tokov, zajetih med KM mikroskopiranjem, smo lahko izračunali vrednosti uporov na stikih elektrod in na plasteh pentacena v kanalu OTT. Rezultati so pokazali, da so strukturne nepravilnosti, ki smo jih opazili že pri meritvah morfologije za vzorce tipa I, krive za velik upor tako na kontaktih kot tudi v plasti pentacena, ki se nahaja v kanalu OTT. Slednji rezultat je bil seveda pričakovan. Bolj zanimiva je bila primerjava KM meritev na vzorcih tipa II in III. Tu se je pokazalo, da je občutno manjša mobilnost na vzorcih tipa II, v primerjavi z vzorci tipa III, posledica večjega upora na meji med izvirno elektrodo in pentacenom.

X. Zivljenjska doba organskih tankoslojnih tranzistorjev: dopiranje s kisikom proti difuziji vode

Izpostavljenost OP atmosferskemu zraku vpliva na njihovo električno in morfološko stabilnost. V nekaterih primerih je opažena degradacija nezaželena, saj vpliva na življenjsko dobo naprav. Po drugi strani pa lahko občutljivost na atmosferske pline izkoristimo za izdelavo senzorjev, ki bazirajo na OP. V obeh primerih je torej pomembno poznavanje vpliva atmosferskih plinov na delovanje OP, zato smo izvedli eksperiment, v katerem smo merili časovne spremembe toka skozi OTT, ki smo jih izpostavili atmosferskemu zraku (Slika 10.1). Te meritve smo povezali z meritvami KM (Slika 10.2).

Pri eksperimentu smo uporabili vzorce, na katerih so bile elektrode narejene s kombinacijo optične in elektronske litografije. Razdalje med elektrodami so bile 4 μ m, dolžina elektrod pa 300 μ m. Elektrode so bile narejene iz 30 nm debele plasti Au. Pod njo je bila naparjena 2 nm debela adhezijska plast Ti. 50 nm debele plasti pentacena so bile naparjene s hitrostjo 2 nm/min, pri temperaturi substrata 60°C.

Rezultati so pokazali, da na tok skozi OTT vplivata dva konkurenčna mehanizma. V začetni fazi je prisotno dopiranje aktivne plasti s kisikom, ki povzroči dodatno akumulacijo naboja in s tem povečanje toka skozi tranzistor. Dodatno se tok poveča še zaradi interakcij med Au elektrodami in kisikom, ki znižajo energijsko bariero za injekcijo naboja iz elektrode v aktivno plast polprevodnika (Slika 10.4 (c)) [122]. Bolj počasno je dopiranje aktivne plasti pentacena z molekulami vođe, ki vnesejo motnje v energijski porazdelitvi stanj, ki so odgovorna za transport naboja po OP. Molekule vođe odigrajo vlogo pasti za naboj, ki teče po polprevodniku, kar privede do zmanjšanja toka skozi OTT, ki smo ga opazili po daljši izpostavljenosti OTT atmosferskemu zraku (Slika 10.1).

Ključne besede

organski polprevodniki, organski tankoslojni tranzistorji, mikrolitografija, vakuumsko naparevanje, mikroskopija na atomsko silo, Kelvinova mikroskopija, upor na elektrodah XVI

Contents

Co	nts	XVII								
1	Intr	roduction		1						
2	Phy 2.1 2.2 2.3	Sics of organic semiconductors General remarks	 	5 5 6 6						
3	3 Charge carrier transport in organic semiconductors									
	3.1	General remarks		9						
	3.2	Polarons		10						
	3.3	Hopping mechanism		12						
	3.4	Multiple trapping and release model		13						
4	Org	anic thin film transistors		15						
	4.1	General remarks		15						
	4.2	OTFT device geometries		15						
	4.3	Components of OTFT		16						
		4.3.1 Gate electrode		16						
		4.3.2 Insulating layer		17						
		4.3.3 Source-drain metallic contacts		17						
	4.4	Operation principle of OTFT		18						
	4.5	Current-voltage characteristic		20						
		4.5.1 Field-effect mobility		22						
		4.5.2 Threshold voltage		24						
		4.5.3 ON/OFF ratio \ldots \ldots \ldots \ldots \ldots		25						
5	Exp	perimental methods		27						
	5.1	Organic molecular beam deposition		27						
	5.2	In situ electrical characterisation		32						

CONTENTS

5	.3 Atomic force microscopy	36 37 38
5	5.3.3 Kelvin force microscopy	39 40 41 42
6 N	Aicrolithography	45
6	.1 Fabrication of chromium mask	46
6	.2 Photoresist	47
	6.2.1 Photoresist and its sensitivity to soft UV light	47
	6.2.2 Operational consideration	48
6	.3 Single layer optical lithography	50
6	.4 Double layer optical lithography	54
6	.5 Single layer electron-beam lithography	57
- T		
	volution of source-drain current as a function of pentacene	50
16	1 Introduction	59 60
7	2 Experimental methods	61
7	3 Besults and discussion	61
7	.4 Conclusion	68
8 N	Morphology of the metal-organic semiconductor contacts:	
\mathbf{t}	he role of substrate surface treatment	69
8	.1 Introduction	70
8	.2 Experimental methods	71
8	.3 Results and discussion	72
8	.4 Conclusions	79
9 (Contact resistance in organic thin film transistors	81
9	1 Introduction	82
9	.2 Experimental $$	83
9	.3 Results and discussion	84
9	.4 Conclusion	91
9	.5 Acknowledgements	91
10 L w	vifetime of organic thin film transistors: oxygen doping vs. vater diffusion	93 94

XVIII

CONTENTS

10.2 Experimental								•		•						95
10.3 Results and discussion								•		•						96
10.4 Conclusion								•		•	•					103
11 Conclusions														105		
Bibliography										109						

XIX

CONTENTS

 $\mathbf{X}\mathbf{X}$

1 Introduction

Organic semiconductors (OSs) have been studied since the late 1940's [1]. Main advantages of OS based devices are low manufacturing cost due to low temperature processing, suitable mechanical properties that allow fabrication of flexible devices and possibility of large area device fabrication. However, despite a large number of experimental and theoretical studies, electronic and optoelectronic devices have started to emerge on market only in recent time.



Figure 1.1: Left image represents Sony's 27-inch prototype organic LCD screens with a 1,000,000 : 1 contrast ratio and with 1080p resolution (full high definition resolution). Top-right image shows the organic light emitting diode (OLED) developed by collaborations of Philips, OSRAM, Siemens, Novaled and Franhofer IPMS. The lifetime of presented OLED is more than 100,000 hours and the price is estimated to be 100 euro per square meter or lower. Bottom-left images represents organic solar cells produced by Konarka technologies. Dimensions of 8 W solar cell presented in the image are 20 cm \times 100 cm.

A huge break trough was made in the mid-1980's, with a feasibility of a low voltage efficient organic light emitting diodes [2]. Further progress has been made in the 1990's, when the pentacene-based organic thin film transistors (OTFTs) reached charge carrier mobility of the order of $1 \text{ cm}^2/\text{Vs}$ [1], which is comparable with the charge carrier mobility in amorphous silicon. Recently, some prototypes e.g. organic solar cells and organic LCD screens emerge on the market (Fig. 1.1).



Figure 1.2: Evolution of OTFT hole mobility for the most common p-type organic semiconductors. Representative range of electron mobility for a-Si:H TFT is shown as a reference. The image was taken from ref. [1]

Fig. 1.2 shows the most important groups of OSs that have been under research from the mid-80's. A tremendous improvement in the charge carrier mobility of various OSs was observed, which is attributed to the synthesis of new organic materials, optimisation of deposition methods and parameters, and optimisation of electrical contacts [1, 3].

Charge carrier mobility is the most decisive parameter that determines the potential use of a given OS in organic electronics. Therefore, a number of experimental methods for extracting the charge carrier mobility were developed. The most commonly used methods are: time of flight method (TOF), space charge limited current method (SCLC) and field effect transistor (FET) method [4]. TOF method is based on measuring the delay-time between the laser pulse, generating the charge inside OS active layer and arrival of the charge to the electric contact [5]. SCLC method is based on measuring the current through the OS, which is placed between two electrodes in a sandwich structured sample. The current through the sample (j) must not be contact limited which means, that ohmic contacts at electrode/OS/electrode interfaces are required. If the latter is fulfilled, the observed current obeys the Child's law, which predicts that $j \propto \mu \cdot U^2/L^3$, where U is the applied voltage, L is the electrode separation, and μ is the charge carrier mobility [4, 6].

In our work, we investigated the electrical properties of the OS pentacene using the FET method. The experimental setup for the FET method is as follows: an organic semiconductor is deposited on top of an insulator with an underlying (gate) electrode, which controls the density of charge, induced at the OS/insulator interface. Charge-injecting source and chargeaccumulating drain electrodes are fabricated either bellow or at the top of an OS active layer. By measuring the current through the source and drain electrodes, the electrical properties of OS layer can be extracted [7]. The electrical characteristics e.g. field-effect mobility, threshold voltage, ON-OFF ratio etc. of OTFTs are influenced by: contact resistance at source/OS and OS/drain interfaces, morphology of OS layer, treatment of insulator surface by self-assembled monolayers, and exposure of OS layer to an ambient air.

Contact resistance at source/OS and OS/drain is an important parameter regarding the performance and optimisation of OTFTs. High contact resistance especially at the source/OS interface can govern the overall charge transport in OTFTs. It is attributed to the charge injection barrier due to the offset between the Fermi energy of electrode and the highest occupied molecular orbital (HOMO) in case of p-type OS and the lowest unoccupied molecular orbital (LUMO) in case of n-type OS [8]. The magnitude of the contact resistance due to the charge injection barrier can be directly observed by applying the Kelvin force microscopy (KFM).

Morphology (the grain size) of OSs layers is also believed to be an important factor in the overall performance of OTFTs. Since, the charge carrier transport in OS crystals depends upon the overlap between molecular orbitals, the density of grain boundaries represent an obstacle for charge transfer between neighbouring grains [9]. Therefore, controlling the grain size is crucial for optimisation of OTFTs. The size of grains in pentacene layers can be tuned by deposition rate and substrate temperature [10]. Morphology of the layers and performance of OTFTs is additionally modified by treating the substrate surface with self-assembled monolayers (SAMs) [11].

Exposure of pentacene based OTFTs to the ambient air degrade their electrical properties (some reports indicate that layer morphology is also changed [12]) due to diffusion of oxygen and water into pentacene layers [13]. The influence of ambient gases to the performance of OTFTs is important from the point of device stability in ambient air as well as from understanding and improving the sensitivity of OSs based gas sensors. Influence of the exposure to ambient air on the performance of OTFTs can be explored by

INTRODUCTION

measuring the current change through the device in a controlled environment (e.g. in vacuum or in N_2 atmosphere) and upon exposure to ambient air.

This thesis is organised as follows: in Chapter 2 electronic structure of OSs is presented as well as more detailed description of pentacene, on which our investigation was focused. Chapter 3 is dedicated to the description of the charge carrier transport phenomena in OSs. Concept of polarons along with two models used to describe the charge transport in OSs are presented.

In Chapter 4, different geometries along with basic components of OTFTs are introduced. Operation and basic parameters of OTFT are also described in more detail.

Chapter 5 is dedicated to the presentation of experimental methods used for the deposition and the morphological characterisation of pentacene layers. In addition, KFM microscopy used for the quantitative mapping of the electric potential between the source-drain electrical contacts and in situ electrical characterisation, is also described. Source-drain electrical contacts, were fabricated by the means of different lithographic processes. Detailed presentation of the materials and techniques, used for fabrication of electrical contacts, will be given in Chapter 6.

In Chapter 7 we present the influence of Ti adhesion layer used in sourcedrain fabrication process on the electric charge transport in OTFTs. In addition, the evolution of I_{sd} and the morphology, as the function of pentacene layer thickness showed that the transport layer is confined in the first-two layers of pentacene.

Correlation of field-effect mobility as a function of deposition rate, substrate temperature and surface treatment is investigated in Chapters 8 and 9. Detailed investigation by in situ electrical measurements, morphological measurements by AFM, and electrical characterisation by KFM showed the importance of contact resistance on the charge transport phenomena in OTFTs.

In Chapter 10 we present the influence of OTFTs exposure to ambient air. Time-depended electric charge transport measurements of pentacenebased OTFTs coupled to KFM, demonstrated that exposure of OTFTs to ambient air results in two competitive mechanisms that are responsible for the variation and in long-term reduction of source-drain current.

2 Physics of organic semiconductors

2.1 General remarks

The performance of OTFTs crucially depends upon the morphology and the crystal structure of OSs layers, due to the π orbital overlap. Both morphology and crystal structure of particular OS can be tuned by different deposition methods and conditions. The choice of the deposition method depends upon physical and chemical properties of OSs, like their vapour pressure and solubility [3].



Figure 2.1: Schematic representation of pentacene molecule (a), which is a typical representative of the small molecular oligomer group of OSs and Poly(3-hexylthiophene-2,5-diyl) (b), which is a typical representative of the polymer group of OSs.

OSs consisting of small molecular oligomers (Fig. 2.1 (a)) are usually prepared by vacuum deposition and tend to pack into the herringbone (e.g. pentacene) or the $\pi - \pi$ stacking structures (e.g. zinc phthalocyanine), which

are governed by the inter-molecular interactions (van der Waals forces and forces between the static quadrupole fields) [3, 14, 15]. The arrangement of molecules in both structures is highly ordered, and as a results high charge carrier mobility is obtained. On the other hand, polymers are soluble in organic solvents, which allows us to use liquid-based layer deposition. Molecular ordering in polymer based OSs is poorer, due to partially cross-linking during the polymerisation process, resulting in poorer charge carrier mobility [16].

Understanding of the inter-molecular electronic structure and the molecular ordering in formation of OSs is crucial for understanding the charge carrier transport phenomena in OTFT devices.

2.2 Electronic structure of organic molecular crystals

OSs are built from electrically neutral molecules. Basic building blocks of molecules consisting OSs are benzene rings, which are comprised from six carbon and six hydrogen atoms. The p_z orbital of each carbon atom is perpendicular to the plane of benzene ring (Fig. 2.2 (a)). Since the distance between carbon atoms is small enough, the overlap between neighbouring p_z atomic orbitals is possible. The result of the overlap is formation of so-called π bonds. The significance of π bonds is formation of delocalised electron density above and bellow the plane of benzene ring. In essence, each electron participating in the π bond is the property of the whole molecule. In contrast, the overlap between neighbouring sp^2 hybrid orbital results in a highly localised electron densities (Fig. 2.2 (b)).

Due to the delocalisation of electronic orbitals the interactions between neighbouring molecules is possible. If the periodicity (structural ordering in the OS) is adequate and the inter-molecular orbital overlap in sufficient, the formation of extended electronic states in OSs appears. The charge transport of positive charge occurs through the highest occupied molecular orbital (HOMO) and the charge transport of negative charge occurs through the lowest unoccupied molecular orbital (LUMO) [17].

2.3 Pentacene

We used pentacene as an active layer in our OTFT devices. It is planar, 1.5 nm long molecule, consisting from 5 benzene rings (Fig. 2.1 (a)) [18].



Figure 2.2: Schematic representation of the sp^2 and p_z atomic orbitals and the σ and π bonds in the benzene ring. Formation of π bonds by overlapping of p_z atomic orbitals, forming an extended π system with an electron density above and below the molecular plane (a). Formation of σ bond by overlapping of sp^2 hybrid orbitals (b).

Pentacene is a p-type semiconductor. Energy gap between HOMO and LUMO level is 2.6 eV [19].

Pentacene has a triclinic crystal structure (Fig. 2.3). Its molecules are arranged into a herringbone structure, which is the result of interplay of interactions between the delocalised π -orbitals, which favour face-to-face π -stacking, and the quadrupolar interaction, which favours edge-to-face packing [15, 20]. The result of low symmetry in pentacene crystal lattice is the anisotropy in the electrical conductivity [21]. The distance between the molecules and their orientation give a good indication about the strength of the orbital overlap. Molecular orbital overlap between neighbouring molecules within a molecular plane (ab-plane; Fig. 2.3 (b)) is larger compared to the orbital overlap between molecules perpendicular to the plane (Fig. 2.3 (a)), resulting in higher conductivity within the ab-plane than between plains.

Fig. 2.3 (a) shows that pentacene molecules are standing almost upright within each monolayer and also at the top of most insulator surfaces (e.g. SiO₂) used in OTFT devices [22, 23]. Two crystalline phases are known in vacuum evaporated pentacene layers. So-called "thin-film phase" is observed in the beginning stages of layer growth up to the certain critical thickness, which depends upon the deposition parameters. The morphology of pentacene thin film phase is characterised by grains assembled from 1.55 nm high terraces. Above the critical layer thickness (~ 40 nm), a second crystalline phase of pentacene is observed, the so-called "bulk phase". The morphology of pentacene bulk phase is characterised by lamellar-like structures. The inter-layer spacing in pentacene bulk phase is 1.45 nm. Measurements show that the thin-film phase favours the charge carrier transport with respect



Figure 2.3: Schematic representation of pentacene crystal structure (a) along the a-axis showing the layered organisation of pentacene thin films (unit cell is also indicated in image), (b) top view, showing a herringbone configuration. The image was taken from ref. [20]

to the bulk phase. This is because in the bulk phase, the π -orbital overlap at the grain boundaries is relatively weak, hindering thereby inter-granular charge carrier transport [24].

3 Charge carrier transport in organic semiconductors

3.1 General remarks

Physical processes governing the charge carrier transport in OSs have been a matter of several investigations [4, 16, 17, 25–28]. Models proposed to explain the charge transport characteristics in OSs are usually based on models developed for the inorganic semiconductors (IOs), since the temperature and electric filed dependence of charge carrier motion in OSs is very often similar to the dependence observed in IOs [26, 29–32].

There are two extreme types of charge carrier transport in semiconductors. The first type is so-called band transport, where charge carriers move as a delocalised plane waves described by a Bloch formalism in a broad carrier band [33]. In the second type charge carriers are highly localised and move from site to site by hopping [34]. In the case of band-transport the charge carrier mobility is $\mu \gg 1 \text{ cm}^2/\text{Vs}$ and the temperature dependence is described as $\mu \propto T^{-n}$, n > 1. In the second case mobility is $\mu < 1 \text{ cm}^2/\text{Vs}$ and the temperature dependence is described as $\mu \propto \exp(-E/kT)$, where Eis the activation energy and k is Boltzmann constant.

Reports show that in OSs both types of transport are observed. In disordered OSs, like in the case of conjugated polymers, charge carrier transport is described by hopping between localised sites [16, 29, 30, 35, 36]. Since the hopping is assisted by phonons, charge carrier mobility increases with temperature, but remains relatively low ($\mu < 1 \text{ cm}^2/\text{Vs}$). On the contrary, in highly ordered organic molecular single crystals, consisting of small oligomers (e.g. naphthalene), band-like transport becomes the prevailing charge transport mechanism. For example, TOF experiments showed that the mobility in single crystal naphthalene measured at T = 4.2 K, may reach values as high as 400 cm²/Vs [32, 37].

Reported values of field-effect mobility in e.g. pentacene polycrystalline OSs are $\mu \sim 1 \text{ cm}^2/\text{Vs}$ [11, 38]. These values fall in to the intermediate range

10CHARGE CARRIER TRANSPORT IN ORGANIC SEMICONDUCTORS

and give no decisive answer about the type of transport mechanism. Furthermore, the experiment performed by Nelson *et al.* [39] on pentacene-based OTFTs, showed that the variation of field-effect mobility with temperature differs between the samples in spite of fabricating the OTFTs under similar conditions. Measured field-effect mobilities as a function of temperature presented in Fig. 3.1, showed thermally activated (Fig. 3.1 (a) and (b)) as well as temperature independent (Fig. 3.1 (c)).



Figure 3.1: Field-effect mobility vs temperature for three different pentacene OTFTs fabricated under similar conditions [39].

3.2 Polarons

Significant property of OSs is a weak Van der Waals intermolecular bond. Weak coupling between neighbouring molecules in OSs leads to a strong localisation of excess charge carriers, which leads to polarisation of surroundings. Polarisation, along with a charge carrier form a quasi-particle called "polaron". Formation of polarons is significant for a charge carrier transport in OSs, since it lowers the energy of charge carriers [40].

One type of polarisation arises from the interaction between a charge carrier and π electrons of surrounding molecules in OSs. The process is called electronic polarisation and the resulting charge carriers are called "electronic polarons" (Fig. 3.2 (a)). Occurrence of electronic polarisation is possible, if



Figure 3.2: (a),(b),(c) show a schematic representation of electronic polarisation, molecular polarisation and lattice polarisation, respectively. By the images, typical relaxation times for particular polarisation are indicated along with typical interaction energies. Dashed lines in (b) and (c) symbolise the size and the position of the molecules before the relaxation processes while the solid lines indicates the size and position of the molecules after the relaxation processes.

a charge carrier between successive hops spends enough time on a particular molecule in OSs to induce the displacement of π orbitals in surrounding molecules. The time needed for inducing dipoles τ_e ranges between 10^{-16} s and 10^{-15} s, which is significantly faster than the typical hopping time in OSs

which $\sim 10^{-14}$ s. Electronic polarisation is a dominant type of interaction of an excess charge carrier with the surrounding lattice in OSs. Typical energy of electronic polarisation is between 1.5 and 2 eV.

Interactions between excess charge carriers and molecular phonons (Fig. 3.2 (b)) lead to formation of "molecular polarons". The intra-molecular vibronic relaxation time τ_v is longer compared to electronic polarisation time τ_e and is comparable with hopping time in OSs. Typical interaction energy caused by formation of molecular polarons ranges between 10 mV and 100 mV.

Interactions can also occur between excess charge carriers and OSs lattice, leading to perturbation of position of atomic nuclei (lattice polarisation) (Fig. 3.2 (c)). Lattice polarisation (τ_l) is slower compared to hopping time, ranging between 10^{-12} s and 10^{-11} s, and thou not very significant for charge transport in OSs. Interaction energy caused by lattice polarisation is of the order of ~ 10 mV.

3.3 Hopping mechanism

Hopping mechanism is a type of charge transport, where the charge carriers hop between the localised states, which are result of structural defects and impurities in OSs [17, 41–43]. In the approach considered by Bässler *et al.* [28], hopping is described by eq. (3.1):

$$\nu_{ij} = \nu_0 \exp\left(-2\gamma a \frac{\Delta R_{ij}}{a}\right) \begin{cases} \exp\left(-\frac{\epsilon_j - \epsilon_i}{kT}\right), & \epsilon_j > \epsilon_i, \\ 1, & \epsilon_j < \epsilon_i. \end{cases}$$
(3.1)

where a is the average lattice distance, $2\gamma a = \Gamma$ is the parameter describing orbital overlap, ΔR_{ij} is the distance between the localised states and $\epsilon_j - \epsilon_i$ is the difference in electronic site energies a carrier has to overcome in order to hop. The relation indicates that better orbital overlap, shorter distance between localised states and smaller energy barrier between localised states lead to higher jump rate and thus better charge carrier transport.

The main feature of hopping mechanism is the temperature dependence of the charge carrier mobility. The mobility increases with the increasing temperature, which indicates that the hopping mechanism is phonon-assisted charge carrier transport. Hopping mechanism was first introduced to explain the transport charge mechanism in amorphous silicon. Temperature dependent drift mobility measurements in amorphous silicon showed three distinct temperature dependant mobility regions. The charge transport in temperature region between 240 K and 200 K was explained by phonon-assisted hopping between localised states [31].

3.4 Multiple trapping and release model

The multiple-trapping-and-release-model (MTR) predicts that the charge transport occurs in extended states, but that most of charge carriers, injected-to the active semiconductor layer are trapped in the localised states which are present in the forbidden energy band and thermally released back to the extended states [25, 26, 31]. The origin of localised states are irregularities in crystal structure, impurities and polarons. MTR was first used to explain the gate voltage dependent mobility [44] and the temperature dependence of a drift mobility in amorphous silicon for certain temperature intervals [31].

Some OSs show high structural ordering and a sufficient inter-molecular orbital overlap, therefore, formation of extended electronic states in these OSs is possible. On the other hand, structural irregularities, impurities and formation of polarons lead to the formation of localised states, with discrete energy levels and characteristic trapping time of a charge carrier. We can distinguish two possibilities: if the trapping time is longer than typical experimental time, the trapped charge carriers (deep-level traps) don't contribute to the mobile charge carriers and to the magnitude of the current. Nevertheless, they alter the electric field and thereby effect the charge transport. On the contrary, when trapping time of charge carriers is short and the energy of localised sites is close to the conductive band (shallow-level traps), charge carriers may become thermally activated and contribute to the overall current [45].

Because of the formation of extended electronic states and the presence of localised sites near the conductive band edge in some OSs, the MTR is often used to explain the charge carrier transport characteristics in OSs: e.g. temperature dependence of the filed-effect mobility in sexithiophene-based OTFTs [26] and the gate voltage dependent field-effect mobility in pentaceneand thiophene-based OTFTs [46, 47]. Temperature and gate voltage dependence of the field-effect mobility in sexithiophene-based OTFTs is presented in the experiment performed by Horowitz *et al.* [26] (Fig. 3.3). The gate voltage dependence of the field-effect mobility is ascribed to a different charge carrier density at the insulator/semiconductor interface, induced by different gate voltages [26] and the temperature dependence is ascribed to a release of trapped carriers in the localised states near the conducting band, which is a thermally controlled activation process [25]. The charge carrier mobility μ predicted by the MTR is related to the mobility in delocalised band μ_0 by:

$$\mu = \mu_0 \alpha \exp\left(-\frac{E_t}{kT}\right) \tag{3.2}$$

where E_t corresponds to the energy difference between trap level and the

delocalised band edge and α is the ration between the effective density of states at the delocalised band edge and the concentration of traps (localised states) [25].



Figure 3.3: Field-effect mobility of sexithiophene based OTFTs vs temperature. Different curves correspond to different gate voltages applied to transistor [26].

We note that hopping and MTR describe conceptually different transport mechanisms. Nevertheless, predicted behaviour of e.g. temperature dependence of mobility is very difficult to differentiate experimentally.
4 Organic thin film transistors

4.1 General remarks

Field-effect transistor is an electronic device that relies on the electric field to control a current through the "conductive channel" in a semiconducting material. When the active layer is fabricated from OSs, the device is referred to as the organic field-effect transistor. The most common configuration of an organic field-effect transistor is organic thin film transistor (OTFT).

Applicability of OTFTs is divided in two segments: firstly, OTFTs are employed for investigation of the basic OS properties (e.g. field-effect mobility, ON/OFF ratio, degradation effects after prolong operation etc.) and secondly, OTFTs can be used as switching or sensing devices in organic electronic applications.

4.2 OTFT device geometries

The most commonly used geometries in OTFTs are the top-contact, bottomgate (TB) (Fig. 4.1 (a)) and the bottom-contact, bottom-gate (BB) (Fig. 4.1 (b)) transistor geometries [48]. In BB transistor geometry, an insulator is separating the gate contact from an OS layer and the source-drain electrical contacts, which are fabricated prior to a deposition of an OS layer by a lithographic process (e.g. optical or electron beam lithography; issue of a contact fabrication will be discussed in the chapter 6). When TB transistor geometry is employed, an OS layer is deposited prior to fabrication of sourcedrain contacts. In the latter, source-drain contacts are usually fabricated by evaporating the desired material (usually metal) through the shadow mask (Shadow-mask technique) [49].

The main advantages of the BB transistor geometry are smaller separation between source and drain contacts (so-called channel length) and fabrication of the source-drain contacts prior to the OS deposition. Therefore, despite of the inferior electrical characteristic compared to the TB transistor geometry



Figure 4.1: Schematic representation of (a) top-contact, bottom-gate TFT device geometry (a) and bottom-contact, bottom-gate TFT device geometry (b). Different colours show different components of OTFTs.

[50, 51], BB transistor geometry is frequently used in experimental work. Since the source-drain electrical contacts are fabricated prior to deposition of OS, the electrical characterisation can take place during the deposition of OS, and so the evolution of charge transport during the growth of OS layers can be observed [52, 53].

4.3 Components of OTFT

Basic components of OTFTs are: gate electrode, insulating layer, sourcedrain electrical contacts and OS active layer. OSs were described in Chapters 2. and 3. The other components will be described in the continuation of this section.

4.3.1 Gate electrode

Density of charge carriers that are present in the semiconductor active layer is controlled by the voltage applied to the gate electrode. In many cases, gate electrode also serves as a substrate on which OTFTs are fabricated.

Materials used for fabrication of gate electrodes are different metals and conductive polymers (e.g. PEDOT:PSS [54, 55]). Despite the variety of materials suitable for gate contact fabrication the most often choice is highly doped silicon, due to the straightforward fabrication of SiO_2 at the top of silicon wafers, which is often used as an insulator in OTFTs [1, 3].

4.3.2 Insulating layer

The primary function of an insulating layer is prevention of current leakage between gate electrode and source-drain electrodes and OS layer. Basic characteristics of insulating layer used in OTFTs devices are: high dielectric constant, high breakdown electric field and low surface roughness.

Dielectric constant is connected with the value of capacitance for particular insulator, and therefore, with the charge induced at the insulator/semiconductor interface. Higher values of a dielectric constant lead to a higher amount of charge induced at the interface without increasing the voltage. Typical values of dielectric constants for insulators used in OTFTs range between 3 and 23.

Breakdown electric field is the maximal electric field that an insulator can sustain before the current through an insulator is observed. The value is used to calculate the minimal thickness of an insulator that still sustains the applied gate voltage. Values of breakdown electric field for insulators used in OTFTs range between 0.1 MV/cm and 8 MV/cm [56–58].

Studies showed that the surface roughness influences the morphology of OSs, and therefore, the performance of OTFTs. When OSs are deposited over the rough surfaces the nucleation density is high, meaning that the grain boundary density is also high. Grain boundaries act as trapping sites for the mobile charge carriers, therefore reducing the performance of OTFTs. Values of surface roughness for insulators used in OTFTs range between 0.2 nm and 0.5 nm [58, 59].

Various inorganic materials (e.g. SiO_2 , SiN_x , Al_2O_3 and Ta_2O_5 [56–59]) and organic materials (e.g. polymethylmethacrylate (PMMA) [60] and polyacrylonitrile (PAN) [61]) have been evaluated as insulating layers for OTFTs. Despite the wide range of available dielectric materials, SiO_2 is by far most often used insulator in OTFTs.

4.3.3 Source-drain metallic contacts

The function of source-drain contacts in OTFTs devices is injection of charge carriers at the source electrode in to the active layer of OS and collection of the charge carriers on the opposite site of OS by the drain electrode. In the case of an n-channel transistor the charge carriers are electrons and must be injected into LUMO state of OS and in the case of p-channel transistor the charge carriers are holes and must be injected into HOMO state of OS, therefore, contacts must be fabricated, using the materials with a proper work function to minimise the energy barrier at the source/OS interface.

The materials usually employed for the source-drain contact fabrication

are metals with a high work function (e.g. Au, Ag, Cr and Pd). In recent years due to the increasing efforts to manufacture all-organic OTFTs, conducting polymers are also used for source-drain contact fabrication (e.g. polyaniline [54], PEDOT [62]).

The main issue of a source-drain contacts fabrication is achieving sufficiently small channel length. The most common techniques used for contacts fabrication are: different methods of lithography, printing or by depositing the material trough the shadow mask. Most frequently used are optical lithographic techniques [49], due to the large range of achievable feature sizes ranging from 50 μ m down to 45 nm [63].

4.4 Operation principle of OTFT

OTFTs are primarily operated as accumulation mode transistors [7]. In the following discussion of OTFT operation the example of p-type OS will be implied.

Voltage is applied to the gate (V_g) and to the drain electrodes (V_d) , while the source electrode is grounded $(V_s = 0 \text{ V})$. The potential difference between the gate and the source electrodes is referred to as the gate voltage (V_g) and the potential difference between the drain and source electrodes is referred to as source-drain voltage (V_{sd}) (Fig. 4.2 (a)). The source is charge-injecting electrode and is more positive than the gate electrode. However, in some cases, due to unintentional doping, surface treatment etc., the accumulation of positive charge at the insulator/semiconductor can be observed even for positive gate voltages. Further discussion on this subject is presented in Section 4.5.2 and in Chapter 10.

In Fig. 4.2 (b-d) basics operating regimes of OTFTs are presented [15, 27]. The result of negative V_g will be accumulation of holes (positive charges) at the insulator/semiconductor interface. The charge density is proportional to the magnitude of the V_g and to the capacitance of the insulator (C_i) . Not all of the accumulated charge is mobile, and therefore, will not contribute to the current through the transistor. Some of the charge will be trapped due to the presence of electrically active structural defects and chemical impurities. These deep traps must be filled, before the current trough the transistor is possible. In other words, V_g more negative than a certain offset voltage, called threshold voltage (V_{th}) , must be applied to the gate electrode. The presence of deep traps reduce V_g to the effective gate voltage $(V_g - V_{th})$.

Fig. 4.2 (b) shows the situation, when no V_d bias is applied to the drain contact and the negative V_g voltage is applied to the gate contact $(V_s = V_d = 0 \text{ V}; V_g < 0 \text{ V})$. In this case, the (positive) charge carrier concen-



Figure 4.2: Schematic representation of OTFTs operating in different regimes. (a) indicates voltages applied to transistor: source voltage (V_s) , drain voltage (V_g) and gate voltage (V_g) . Channel length (l) is the distance between the source and drain contacts and channel width (W) is the length of source and drain contacts. (b) shows the situation, when $V_d = 0$ V and negative V_g is applied to the gate contact. (c) shows the "linear regime" of OTFT operation (d) shows the "saturation regime" of OTFT operation.

tration in the transistor is uniform across the transistor channel. A linear gradient of charge is formed, when a small negative V_d bias is applied to the drain contact ($(V_d < 0 \text{ V}; V_d > (V_g - V_{th}))$ (Fig. 4.2 (b)), resulting in a current flow through the transistor, which is proportional to the source-drain

voltage (V_{sd}) . The mode of transistor operation under these conditions is referred to as "linear regime" of transistor operation. This regime persists approximately up to the point $V_d \sim (V_g - V_{th})$ at which the depletion region next to the drain contact starts forming (pinch-off point) (Fig. 4.2 (c)). The depletion region forms because the electric potential inside the transistor channel near the drain contact is above the threshold voltage, therefore only the space-charge limited current can flow across the saturation region. Further decrease of V_d will not increase the current flow trough the transistor, but will only increase the expansion of the depletion region towards the source contact (Fig. 4.2 (d)). The mode of transistor operation under $V_d < (V_g - V_{th})$ conditions is referred to as "saturation regime" of transistor operation.

4.5 Current-voltage characteristic

Current density (j) in a semiconductor depends upon a charge carrier density n and average velocity $\langle v \rangle$ induced by an electric field E parallel to the charge carrier motion $(j = e_0 n \langle v \rangle)$ [4, 33]. The magnitude of j can be controlled by e.g. electric field applied to the gate contact (section 4.4). On the other hand, the relation between $\langle v \rangle$ and electric field is linear $(\langle v \rangle = \mu E)$, with a proportional coefficient charge carrier mobility (μ) , which is the intrinsic electronic transport quantity that is specific for a given semiconductor material.

Operation of OTFTs in different regimes presented in Section 4.4 can be described analytically. Analytical approach is only possible, by assuming the gradual channel approximation, which means that the electric field induced by the gate voltage, perpendicular to the current flow, is much higher than the electric field induced by the drain voltage [64, 65]. In addition, ohmic contacts and no voltage drop at source/semiconductor and semiconductor/drain interfaces will be assumed [15, 27].

When voltage is applied to the gate electrode, the charge is induced at the semiconductor/insulator interface, given by:

$$q = C_i \cdot V_g, \tag{4.1}$$

where q is the induced charge per unit area and C_i is the capacitance per unit area of an insulator. We indicated in the section 4.4 that not all the charge, induced by applying V_g , is mobile. Therefore, the surface density of the mobile charge q_{mob} is given by:

$$q_{mob} = C_i (V_g - V_{th}). \tag{4.2}$$

In eq. (4.2) the V_d is assumed to be 0. When V_d is applied to the drain contact, potential difference between V_g and transistor channel vary along the channel. Therefore, the charge density at certain point x in the transistor channel is given by:

$$q_{mob} = C_i (V_g - V_{th} - V(x)), \tag{4.3}$$

where x = 0 at the source/semiconductor interface. By neglecting the diffusion current (assuming that only the charge carriers induced by V_g , participate to the transistor current) the current trough the transistor (I_d) can be presented by:

$$I_d = W \mu q_{mob} E_x, \tag{4.4}$$

where W is the channel width, μ is the charge carrier mobility and E_x is the electric field between source and drain contacts. By rewriting E_x as $E_x = dV/dx$ and inserting it along with eq. (4.3) into eq. (4.4), we find:

$$I_{d}dx = w\mu C_{i}(V_{q} - V_{th} - V(x))dV.$$
(4.5)

Next step is integration of eq. (4.5) along the channel from x = 0 to l and from V(x) = 0 (x = 0 at the source contact) to V_{sd} (x = l at the drain contact). When the source electrode is grounded $V_{sd} = V_d$. Integration of eq. (4.5) leads to the relation describing I_d :

$$I_d = \frac{W}{l} \mu C_i \left[(V_g - V_{th}) V_{sd} - \frac{1}{2} V_{sd}^2 \right].$$
(4.6)

Second term $\frac{1}{2}V_{sd}^2$ in eq. (4.6) can be neglected providing that $(|V_{sd}| \ll |(V_g - V_{th})|)$, leading to:

$$I_d = \frac{W}{l} \mu_{lin} C_i \left[(V_g - V_{th}) V_{sd} \right], \qquad (4.7)$$

describing the linear regime of transistor operation, where μ_{lin} is the fieldeffect mobility in the linear regime. By applying $|V_{sd}| > |(V_g - V_{th})|$ the depletion region is formed near the drain contact (section 4.4), therefore V_{sd} can be replaced by the $(V_g - V_{th})$ in eq. (4.6), leading to the relation, describing the I_{sd} in the saturation regime:

$$I_d = \frac{W}{2l} \mu_{sat} C_i \left[(V_g - V_{th})^2 \right].$$
 (4.8)

where μ_{sat} is the field-effect mobility operating in saturation regime. Sourcedrain current-voltage characteristics (I-V characteristics) of operating OTFTs for different V_d and V_g are presented in (Fig. 4.3)



Figure 4.3: Schematic representation of source-drain current-voltage characteristics (I-V characteristics) in OTFTs. Presented characteristics indicates the linear and saturation regimes of OTFTs operation. Characterisation is performed by keeping the gate voltage constant and sweeping the source-drain voltage. Gate voltage is increased from the bottom to top curve, respectively. Data presented in the image are fictitious and are obtained from ref. [27].

4.5.1 Field-effect mobility

One method of measuring the charge carrier mobility in OSs is by measuring the current-voltage (I-V) characteristic of an OTFT, and by doing so, extracting the filed-effect mobility (μ_f) . Measured values of μ_f usually deviate from the intrinsic values of μ for a given OS, due to e.g. the resistance at source/semiconductor and semiconductor/drain interfaces [66]. Nevertheless, OTFTs are often used for the characterisation of OS layers and μ_f is a standard of performance. The value of μ_f is extracted either from the linear $(\mu_{f,lin})$ or saturation regime $(\mu_{f,sat})$ of transistor operation (Fig. 4.3) [15, 27, 67].

For the purposes of calculating the field-effect mobility in the linear regime, eq. (4.7) must be derived with respect to V_g (eq. (4.9)) or with respect to V_{sd} (eq. (4.10)):

$$g_m = \frac{\partial I_d}{\partial V_g} \bigg|_{V_{sd}} = \frac{W}{l} C_i \mu_{f,lin} V_{sd}, \qquad (4.9)$$

$$g_d = \frac{\partial I_d}{\partial V_{sd}} \bigg|_{V_g} = \frac{W}{l} C_i \mu_{f,lin} (V_g - V_{th}), \qquad (4.10)$$

with g_m termed as transconductance and g_d termed as conductance. The value of g_m is calculated by fitting the linear part of the transfer curve presented in Fig. 4.4 (a). By rewriting eq. (4.9), $\mu_{f,lin}$ is extracted:

$$\mu_{f,lin} = g_m \cdot \frac{l}{WC_i V_{sd}} \tag{4.11}$$

The value of g_d is calculated by fitting the I-V characteristics in the linear region (Fig. 4.3). By rewriting eq. (4.10), $\mu_{f,lin}$ of the form:

$$\mu_{f,lin} = g_d \cdot \frac{l}{WC_i(V_g - V_{th})},\tag{4.12}$$

can be extracted. Eq. (4.11) is more general than eq. (4.12), since it is applicable also for gate-voltage-dependent field-effect mobility. In addition, eq. (4.12) contains V_{th} , meaning that the transfer characterisation is required to determine the value of V_{th} .

Field-effect mobility in the saturation regime can be extracted in two ways. First, eq. (4.8) can be directly rewritten as:

$$\mu_{f,sat} = I_{d,sat} \cdot \frac{2l}{WC_i(V_g - V_{th})^2},$$
(4.13)

where $\mu_{f,sat}$ and $I_{d,sat}$ are the field-effect mobility and the source-drain current in the saturation regime, respectively. $I_{d,sat}$ is obtained from an I-V curve (Fig. 4.3) in the saturation regime for a given V_g . $\mu_{f,sat}$ in eq. (4.13) is V_{th} dependent, therefore, transfer characterisation must be performed to determine the value of V_{th} . Second approach of the $\mu_{f,sat}$ extraction is by deriving eq. (4.8) with respect to V_g :

$$\mu_{f,sat}(V_g) = \frac{\partial I_{d,sat}}{\partial V_g} \cdot \frac{l}{WC_i(V_g - V_{th})}.$$
(4.14)

Derivative $\frac{\partial I_{d,sat}}{\partial V_g}$ in eq. (4.14) is obtained from a transfer curve in saturation regime (Fig. 4.4 (b)).

Typical values of field-effect mobility for different OS in OTFTs vary between 10^{-6} cm²/Vs and 2 cm²/Vs [1, 7, 48, 68].



Figure 4.4: Schematic representation of current-voltage characteristics in OTFTs. (a) represents a transfer characteristic in the linear regime $(|V_d| \ll |V_g|)$. (b) represents a transfer characteristic in the saturation regime $(|V_d| \gg |V_g - V_{th}|)$. Threshold voltage V_{th} indicated in the image is obtained by the intersection of the linear fit to the square root of the drain current and the x-axis. Transfer curves were obtained by keeping the source-drain voltage constant and sweeping the gate voltage. Data presented in the image are fictitious and are obtained from ref. [27].

4.5.2 Threshold voltage

Threshold voltage is calculated either from the transfer curve in the linear or in the saturation regime (Fig. 4.4). In the case of using the transfer curve in the linear regime, V_{th} is obtained by fitting the linear part of the transfer curve (Fig. 4.4 (a)), to a linear curve, and extrapolating to the horizontal axis. When transfer curve in the saturation regime is employed, V_{th} is obtained by the intersection of the linear fit to the square root of the I_d and the horizontal axis (Fig. 4.4 (b)).

By considering the future organic electronic applications, it is desired to keep the V_{th} close to 0 V and constant during the device operation. However, measurements performed by McDermott *et al.* [69] on OTFTs, fabricated by depositing pentacene on SiO₂-covered Si substrate, showed a variation in V_{th} in the range from - 10 V to + 10 V. The stability of V_{th} was improved by treating the SiO₂ surface by self-assembled monolayer (SAM), such as octadecylphosphonate 1. After deposition of SAM V_{th} was stabilised to a value of $-6 V \pm 1 V$ [69]. In addition, it was found that different SAMs yield different values of V_{th} . For example phenethyltrichlorosilane yielded $V_{th} = -13 V$ and 1H,1H,2H,2H-perfluorooctyl-trichlorosilane $V_{th} = +26 V$ [70]. V_{th} stability after extended OTFT device operation is also an important issue. Measurements showed shift of V_{th} towards more negative values, after extended (14 hours) OTFTs operation [71], induced by the gate bias stress, which was explained by the long-term trapping and release of charge carriers, caused by structural defects and impurities at the insulator/semiconductor interfaces [72]. In addition, V_{th} shift was also observed after exposing OTFTs to the ambient air. The issue will be discussed in section 10.

4.5.3 ON/OFF ratio

ON/OFF ratio is an important parameter determining the performance of OTFTs. It is the ratio between I_d current in "on"-state at the particular gate voltage (usually $V_g = V_{sd} = -20$ V) and "off"-state ($V_g > 0$ V, for the p-type OS and for $V_{th} < 0$ V) [27]. It can be extracted from the saturation regimes of the transfer curves ($|V_{sd}| \gg |(V_g - V_{th})|$). ON/OFF ratio should be as large as possible for a clean switching behaviour. High ON/OFF ratio is achieved by maximising I_d in the ON state and minimising I_d in the OFF state [15]. High I_d in the ON state is a signature of OTFT with a high field-effect mobility. Low I_d in the OFF state indicates low dopant concentration, generating the parasitic current through the bulk of the OS and low leakage current through the gate insulator. Therefore, the optimisation of OTFTs, leading to higher field-effect mobility, and treating the surface with SAMs, resulting in lower insulator leakage currents [72], would results in higher ON/OFF ratio. Typical values of ON/OFF ratio for different OSs vary between 10^3 and 10^8 [1, 48].

5 Experimental methods

5.1 Organic molecular beam deposition

Organic molecular beam deposition (OMBD) is a technique of OS layer deposition on a variety of substrates. It is based on heating the depositing material above the sublimation temperature (and well below its chemical decomposition temperature) and directing the resulting molecular flux to the substrate surface, which is kept at the appropriate temperature. Main advantages of OMBD are high chemical purity and monolayer control over the OS layer growth [73].

OMBD is realised in a vacuum chamber, where two categories of vacuum can be differentiated. For background pressure (p) ranging between 10^{-1} Pa to 10^{-7} Pa term high vacuum (HV) is used and for p below 10^{-7} Pa, the term ultrahigh vacuum is in use. The characteristic feature of OMBD is the beam nature of the mass flow of the incident molecules towards the substrate [74]. From this point of view it is important to consider the vacuum conditions to preserve the beam nature of the mass flow. The highest value of a background pressure may be estimated from the condition, that the mean free path L_b of depositing molecules must be larger than the distance between the aperture of the beam source and the substrate surface.

By using the kinetic theory of an ideal gas, the expression for the mean free path is given by:

$$L = \frac{1}{\sqrt{2\pi n d^2}},\tag{5.1}$$

where d is the molecular diameter and n is the concentration of the gas molecules in the vacuum. The latter is related to the pressure p and the temperature T by:

$$n = \frac{p}{k_B T},\tag{5.2}$$

where k_B is the Boltzmann constant. The conditions during the layer depo-

sition can be described as a mixture of two gases: the background gas and a gas of depositing molecules. The main free path can be therefore expressed as:

$$L_b^{-1} = \sqrt{2}\pi n_b d_b^{\ 2} + \pi n_g d_{bg}^{\ 2} \sqrt{1 + v_g^{\ 2}/v_b^{\ 2}},\tag{5.3}$$

with

$$d_{bg} = \frac{d_b + d_g}{2},\tag{5.4}$$

where n_b , d_b and v_b are the concentration, the diameter and the average velocity of the molecules in the molecular beam, respectively, and n_g , d_g and v_g are the concentration, the diameter and the average velocity of the molecules of the background gas. A partial pressure of the background gas is obtained by inserting eq. (5.4) in eq. (5.3) and rearranging eq. (5.3):

$$p_g = k_B T \frac{L_b^{-1} - \sqrt{2\pi n_b d_b^2}}{\pi d_{bg}^2 \sqrt{1 + v_g^2 / v_b^2}}.$$
(5.5)

The maximum value of the background pressure (p_g) for pentacene is calculated by applying the following parameters [18, 74, 75]:

$$T_b = 450$$
K, $v_b = 200$ m/s, $L_d = 0.2$ m, $d_b = 10^{-9}$ m, $n_b = 2 \cdot 10^{14}$ m⁻³
 $T_g = 300$ K, $v_g = 510$ m/s, $d_g = 3.7 \cdot 10^{-10}$ m

Maximum value of background pressure calculated with above values is $p_{g,max} = 5 \cdot 10^{-3}$ Pa. This result indicates, that the beam nature of the mass transport is preserved in HV conditions.

More rigorous demand regarding the background pressure is connected with the purity of deposited layers. Namely, the degree of impurity incorporation in semiconductor layers depends on the quality of the vacuum. Therefore, the impurity incorporation rate should be substantially lower than the layer growth rate. The quantity, determining the magnitude of impurity incorporation is the time in which a monolayer of background gas atoms is formed on a substrate surface (τ). By using the kinetic theory of gasses, τ is estimated by [73]:

$$\tau = \frac{N_s \zeta (2\pi m k T)^{1/2}}{p_g},$$
(5.6)

where N_s is the density of surface atoms required to form a complete monolayer, ζ is the atomic sticking coefficient and p_g is the value of background pressure. τ can be estimated by assuming, that the principal background gas in a vacuum is N_2 and that the $N_s = 10^{14}$ molecules/cm². The upper limit of τ is obtained by applying $\zeta = 1$. By using eq. (5.6) and e.g. background pressure $p = 10^{-6}$ Pa, time in which a monolayer of background gas atoms is formed on a substrate surface is $\tau \sim 6$ min.

Initial stages of film growth are classified in three categories (Fig. 5.1): layer-by-layer (Frank-van der Merwe), island (Volmer-Weber) and layer-plusisland (Stranski-Krastonov) [73, 74].



Figure 5.1: Schematic representation of three modes of OMBD growth: layer-by-layer (Frank-van der Merwe), island (Volmer-Weber) and layer-plus-island (Stranski-Krastanov) growth, from the top to the bottom, respectively. The image was taken from ref. [75].

In the case of island growth, clusters of molecules nucleate on a substrate and then grow into islands, without forming a complete layer (three dimensional growth). Island growth is observed, when an attractive inter-molecular interaction between depositing molecules is stronger than an interaction with a substrate surface. Layer-by-layer growth is observed, when the molecules are more strongly bound to a substrate than to each other, so that molecules form a complete monolayer on a surface, which becomes covered with a less tightly bound second layer. The layer-plus-island growth mode is an intermediate case. After forming the first (or almost complete) monolayer, islands are formed on top of the existing layer. This is the growth mode usually observed, during pentacene growth on SiO₂ substrate, for deposition rate ranging between 0.5 nm/min and 50 nm/min and for substrate temperature ranging between 300 K and 360 K [76].

The molecules, arriving at the substrate surface, can undergo a series of processes on the surface (Fig. 5.2) [74, 75]. They can be re-evaporated from the surface, releasing the energy E_a in the process. They can diffuse on the substrate surface, with the diffusion energy E_d , until an energetically favourable site is reached.



Figure 5.2: Schematic representation of surface processes during the OMBD. The image was taken from ref. [75].

Such sites can be structural defects on the substrate or already existing islands. Stable islands are formed, when the minimum number of molecules is contained inside an island. Theoretical treatment of the initial stages of layer growth by Ruiz *et al.* [77] predicts that the number of molecules *i* required to form a stable island of pentacene on SiO₂ is 2 and reports by Pratontep *et al.* [78] predicts i = 3. The density of stable islands N depends on the deposition rate κ and on the substrate temperature T_s according to:

$$N \propto \kappa^{\delta} \exp(\beta E_N),$$
 (5.7)

where δ is the function of *i*. E_N is a function of E_i , E_a and E_d and its value varies for different theoretical approaches, and $\beta = (k_B T_s)^{-1}$ [74–78]. Eq. (5.7) shows that higher deposition rate κ results in higher island density and higher substrate temperature T_s results in lower island density.

We performed the deposition of OS layers in a vacuum system presented in Fig. 5.3. The vacuum inside the chamber was achieved by a rotary backing pump E2M1.5 (Boc Edwards) and a turbomolecular pump EXT255H (Boc Edwards). The background pressure ranged between $5 \cdot 10^{-5}$ Pa and 10^{-6} Pa. The semiconductor used in our work was pentacene, supplied by Fluka and Rieldel-de-Haën. Pentacene powder was placed in temperature controlled effusion cells. The flux of semiconductor molecules was controlled by the temperature inside the effusion cell ranging between 125° C to 175° C. The thickness of pentacene layers was measured with thickness monitor, with the resolution of 2 A. The sample was placed inside the vacuum chamber on the custom-made sample holder (Fig. 5.4 (a)), which was attached on the electrical feedthrough (Caburn MDC) (Fig. 5.4 (b)). The temperature of the sample was controlled by a kapton flexible heater (Omega Engineering, Inc.) (Fig. 5.4 (d)) and measured with the Pt-100 temperature sensor (Heraeus Sensor Technology) (Fig. 5.4 (c)). We estimated the precision of the sample temperature to $\pm 3^{\circ}$ C.

Sample holder enable us to connect the source-drain and gate contacts

with the electrical feedthrough, which was connected with the measuring instruments outside the vacuum chamber. This setup allowed us to measure the evolution of electric current during the deposition of pentacene active layer from the initial stages of layer growth up to thicker layers, as well as in situ electrical characterisation of thick pentacene layers. By controlling the molecular flux and the substrate temperature, we were able to investigate in situ the influence of deposition conditions on electrical performance of pentacene based OTFTs. Deposition of pentacene layers was performed in our laboratory in Ajdovščina.



vacuum chamber

Figure 5.3: Setup of our in situ experiment. Samples were put inside the vacuum chamber and connected with a power supply and an ammeter outside the chamber. When the mechanical shutter was removed, an OS reached the sample and the measurement began.



Figure 5.4: Samples were placed into custom-made sample holder (a), which was attached on an electrical feedthrough (b). The sample temperature was measured with the Pt-100 temperature sensor (c) and controlled by a kapton flexible heater (d).

5.2 In situ electrical characterisation of thick pentacene layers

After the pentacene layer deposition, the in situ electrical characterisation of OTFTs was performed. At this point, we will present results of the electrical

characterisation of a typical OTFT device prepared in our experiment.

I-V characterisation of an OTFT with a channel length $l = 4 \ \mu \text{m}$ and a channel width $W = 300 \ \mu \text{m}$, was performed by sweeping V_{sd} between 5 V and -25 V. V_g ranged between 0 V and -30 V. Presented results in Fig. 5.5 show the linear regime at low V_{sd} according to eq. (4.7) and saturation regime at $V_{sd} \sim |V_g - V_{th}|$ according to eq. (4.8).



Figure 5.5: Results of I-V characterisation of a typical OTFT device prepared in our experiment. I_{sd} was measured by sweeping the V_{sd} between 5 V and -25 V (for the purpose of better clarity, only the values between 0 and -25 V are presented in the image) at constant V_g . V_g was increased between 0 V and -30 V by the 5 V step. Again, owing to better clarity, only the measurement for V_g : 0 V, -15 V, -20 V, -25 V and -30 V are presented from the top to bottom curve, respectively.

Transfer characteristics of an OTFT in linear and saturation regime are presented in Fig. 5.6 (a) and Fig. 5.6 (b), respectively.

Measurement of transfer characterisations in linear regime was performed by keeping constant $V_{sd} = -1$ V and sweeping V_g between 5 V and -25 V. By fitting the linear part of the transfer curve (Fig. 5.6 (a)), to a linear curve, and extrapolating to the horizontal axis, we have found the value of $V_{th} = -11.3$ V. The value of V_{th} was found to vary significantly between the samples. V_{th} observed in our experiments varied between -15 V and +5 V. Varying of V_{th} was attributed to the influence of trap sites formed at the SiO₂/pentacene interface and at the grain boundaries, owing to the chemical reactions between SiO₂, and water and oxygen molecules [79]. The same



Figure 5.6: Current-voltage characterisation of a typical OTFT device prepared in our experiment. (a) represents a transfer characteristic in the linear regime ($|V_d| \ll |V_g|$). Threshold voltage was extracted by fitting the measurements in the linear part of the transfer curve and cross-section of x-axis (indicated with arrow). (b) represents a transfer characteristic in saturation regime ($|V_d| \sim |V_g - V_t|$). ON/OFF ratio was obtained by dividing the I_{sd} current in ON state ($V_g = -25$ V and $V_{sd} = -20$ V) and in OFF state ($V_g > V_{ON}$ V and $V_{sd} = -20$ V).

behaviour of the pentacene OTFTs fabricated on the untreated Si/SiO₂ substrates was reported also by McDermott *et al.* [69]. The significant improvement in V_{th} stability was achieved by treating the SiO₂ surface with SAMs, and thereby, reducing the charge trap density at the pentacene/insulator interface.

Measurement of transfer characterisations in saturation regime was performed by keeping constant $V_{sd} = -20$ V and sweeping V_q between 5 V and -25 V. Transfer characterisation at $V_{sd} = -20$ V was significant for obtaining the ON/OFF ratio. Current flow through OTFTs was observed after applying a certain voltage to the gate contact, so-called on-voltage (V_{ON}) (Fig. 5.6 (b), indicated with arrow), after which, abrupt increase (indicated with the steep slope) in I_{sd} was observed. At this poin, transistors operated in the sub-threshold-voltage regime. When V_g was increased, reaching the value $|V_q - V_{th}| \sim |V_{sd}|$, OTFTs operated in the saturation regime (indicated with the levelled slope). Further increase in V_g would lead to $|V_g - V_{th}| \gg |V_{sd}|$ and to the linear regime of transistor operation. This regime was rarely reached for $V_{sd} = -20$ V, due to high V_q and thus possibility of damaging OTFTs. The OFF current was measured for $|V_g| > |V_{ON}|$ and the ON current for $V_q = -25$ V. Relation of both was used for extracting the ON/OFF ratio, which was estimated to be $5 \cdot 10^3$ (Fig. 5.6 (b)). Values of ON/OFF ratio, observed in our experiments, varied between 10^3 and 10^5 , and dependent on the leakage current through the SiO_2 insulator (increasing the OFF current; decreasing the ON/OFF ratio) and on the overall transistor performance (increasing the ON current; increasing the ON/OFF ratio), e.g. relatively low ON/OFF ratio, measured in the pertinent OTFT, was attributed to the relatively high leakage current through the SiO_2 insulator.

Field-effect mobilities of OTFTs were calculated by using eq. (4.13). $I_{d,sat}$ was extracted from I-V measurements in the saturation regime (Fig. 5.5). By applying the value of $V_{th} = -11.3$ V, $C_i = 10$ nF/cm² for 200 nm thick SiO₂ and W/l = 75 for the pertinent OTFT, the field-effect mobility at $V_g = -15$ V was $\mu_{sat} = 0.035$ cm²/Vs. Values of field-effect mobility measured in our experiment, varied between 10^{-4} cm²/Vs and 0.25 cm²/Vs. The observed difference in field-effect mobility was attributed to the different deposition conditions (e.g. different deposition rates and substrate temperatures) and to the impact of different lithographic methods used in source-drain contact fabrication process.

Electrical characterisation of OTFTs was performed in our laboratory in Ajdovščina.

5.3 Atomic force microscopy

After the pentacene layer deposition, the morphology and additional electrical characterisation was performed ex situ, by the atomic force microscopy (AFM). We used Veeco CP-II atomic force microscope (Veeco Instruments) in our work. The measurements were performed in our laboratory in Ajdovščina.

The basic idea of AFM is measuring a force between a sharp tip and the sample surface. The tip is mounted at the end of a cantilever. Radius of a tip is usually less than 10 nm, while the length of cantilever ranges between 100 μ m and 200 μ m [80]. Static deflection of the cantilever or change in its dynamic properties due to the interaction between the tip and the sample surface can be exploited for the surface investigation (Fig. 5.7) [81].



Figure 5.7: Schematic representation of an atomic force microscope. The incident laser beam is reflected from the cantilever to the position sensitive detector, measuring the deflection of the cantilever in the normal direction perpendicular to the sample (z direction). The sample is mounted on a piezoelectric scanner, whose xy movement is controlled by the voltage applied to the scanner and thus allows mapping of the morphological, electrostatic, magnetic... etc. properties of the surface.

Cantilever banding is detected by monitoring the reflection of a laser beam from the top of the cantilever on a position sensitive photodiode (Fig. 5.7). Different forces (e.g. van der Waals forces, electrostatic forces, magnetic forces... etc.) can contribute to the bending of a cantilever and thus different surface properties can be detected.



Figure 5.8: Schematic representation of an interatomic force vs. distance. The image was taken from ref. [82].

Interatomic forces can be attractive or repulsive, depending on the distance between a tip and sample (Fig. 5.8). At small tip-surface separation the principal interaction arises from repulsion of electronic clouds in the tip and on the surface, governed by Pauli exclusion principle. When the tip is further away from the surface (between 1 nm and 10 nm), forces act between dipoles, that arise from fluctuations of electron density and dipoles induced in their electric field, resulting in an attraction between a tip and a surface (van der Waals forces) [81, 82]. Both types of forces can be exploited for investigation of a surface morphology. Electrostatic forces can also act between a tip and a surface. Their strength and distance dependence obey Coulomb's law [81]. Electrostatic forces can be exploited to map the potential distribution on the sample surface.

5.3.1 Contact mode

Contact AFM mode can be used for the morphological investigation of surfaces. It is based upon the measurements of a cantilever deflection. AFM tip is brought into a close contact with a sample surface, so that the repulsive interatomic forces deflect a cantilever (indicated on the left side of Fig. 5.8). In addition, a capillary attractive force is also present. It is exerted by a thin water layer often present on the sample surface in an ambient environment. The magnitude of the capillary force is $\sim 10^{-8}$ N. The equilibrium position of a tip is determined by the equilibrium of both attractive and repulsive forces, balanced by the force, which is exerted by the cantilever it self. The magnitude and sign (repulsive or attractive) of the cantilever force depends upon deflection of a cantilever and upon its spring constant $(k = \frac{df}{dx} > 1 \text{ N/m})$. Magnitude of the total force exerted on the sample surface varies from 10^{-8} N (cantilever pulling away from a surface, almost as hard as a water is pulling down a tip), to the typical operating forces between 10^{-7} N and 10^{-6} N. Resolution of measurements in the z direction (direction of the tip deflection) is of the order of 1 Å. Force inserted by a tip to a sample surface is relatively large, therefore, contact mode is not suitable for morphological investigation of soft organic samples.

5.3.2 Noncontact mode

Noncontact AFM mode is less destructive compared to the contact mode and thou suitable for the morphological surface imaging of soft samples. Therefore, it was the preferred mode of operation in our experiments. In noncontact mode, a cantilever vibrates near a sample surface, with a tip to sample distance ranging between 1 nm to more then 10 nm (indicated on the right side of Fig. 5.8).

Noncontact mode exploits the change in the resonant frequency of a cantilever for morphological measurements of sample surfaces. Resonant frequency ω of a cantilever is given by [82]:

$$\omega = \sqrt{\frac{k_{eff}}{m}},\tag{5.8}$$

where k_{eff} is the effective cantilever constant and m is the mass of a cantilever. Effective cantilever constant is the sum of two terms:

$$k_{eff} = k - f', \tag{5.9}$$

where k is the cantilever spring constant far from a sample surface, depending only on the cantilever dimensions and Young's module. When a cantilever is moved into close proximity of a sample surface, attractive van der Waals forces start acting between a tip and a surface, resulting in the change of cantilever spring constant as indicated in eq. (5.9) due to the force gradient f' between a tip and a sample surface. Magnitude of the van der Waals force is $\sim 10^{12}$ N [82]. Change in a cantilever spring constant results in a shift of the cantilever resonant frequency. If the resonant frequency shifts, then the amplitude of a cantilever vibration at a given frequency changes. This shift in amplitude, associated with a shift in a resonant frequency, is the basis for the amplitude modulation measurement technique, used in our AFM. A feedback mechanism ensures a constant cantilever vibration amplitude by adjusting and restoring the tip to sample distance during a scan. As in contact mode, the amount of z movement necessary to maintain the tip to sample distance is used, to generate a morphological image of a surface. Noncontact mode is at the moment the only operation mode, providing true atomic resolution of the surface imaging [81].

5.3.3 Kelvin force microscopy

Kelvin force microscopy (KFM) technique was named after Lord Kelvin, who first introduced the pioneer technique in 1898, to explain the formation of built-in contact potential differences in metals. When two plates of a capacitor, comprised of different metals are electrically connected, electrons flow from the material with the lower work function towards the material with the higher work function. The electric field in the capacitor induced by these charges, can be extinguished by applying external voltage to the capacitor, which equals the measured contact potential. Kelvin's method was improved by introducing a vibrating reference surface. Mechanical oscillation of a metallic plate at the frequency ω , induces changes in the system capacitance, therefore, inducing the alternating current I(t), given by [83]:

$$I(t) = V\omega\Delta C\cos(\omega t), \tag{5.10}$$

where V is the contact potential difference and ΔC is the difference in capacitance. By measuring the I(t), contact potential difference V can be extracted. Both ideas were adopted and adjusted in order to use the AFM for measuring the electrostatic force between the tip and the sample.

First, when performing the KFM surface investigation, an AFM must work in the noncontact mode. Second, an oscillating potential V_{ac} at frequency ω (which is ~ 5-times smaller than the resonant frequency of a cantilever) and additional voltage bias V_{dc} is applied to a tip. Therefore, the tip can interact electrostatically with a sample surface during the scan, being attracted and repelled at the frequency ω . We used Olympus OMCL-AC240TM-B2 cantilevers (Olympus Corporation), with the resonant frequency 70 kHz and the spring constant 2 N/m.

The voltage difference between the tip and the surface, can be expressed as:

$$V(t) = V_{dc} - V_s + V_{ac}\sin(\omega t), \qquad (5.11)$$

where V_s is the electrical potential at the substrate surface. The signal measured by an AFM, is due to the force between the tip and a substrate surface, meaning, that the voltage difference V(t) must be rearranged in such a manner, to show the connection between the signal V(t), V_s and the cantilever deflection signal. When assuming the parallel-plate geometry, the electrostatic force between a tip and the sample surface can be expressed as:

$$F = q \cdot E = q \cdot \frac{V}{d} = C \cdot \frac{V^2}{d}, \qquad (5.12)$$

where q is the electric charge, C is the capacitance and d is the tip to sample distance. By inserting eq. (5.11) into the last term of eq. (5.12), the following relation is obtained:

$$F(t) = \frac{C}{d} \cdot \left[(V_{dc} - V_s)^2 + \frac{1}{2} V_{ac}^2) \right] + \frac{2C}{d} \cdot (V_{dc} - V_s) \cdot V_{ac} \sin(\omega t) - \frac{C}{2d} \cdot V_{ac}^2 \cos(2\omega t).$$
(5.13)

The total cantilever deflection signal, which represents the force F(t) between the tip and the sample is analysed in terms of three separate signals: the DC part and AC parts with frequencies ω and 2ω . Term important for KFM is AC containing the frequency ω (AC ω term). This part of F(t) signal is isolated by sending the signal to a lock-in amplifier. Amplitude of the AC ω signal can be brought to zero, by applying the DC offset potential (V_{dc}) that matches the surface potential V_s . A feedback loop can be added to the system hardware, to vary the V_{dc} so that the output of the lock-in amplifier of the AC ω signal is zero. The magnitude of V_{dc} can be therefore directly used to generate 2D image of an electric potential on a substrate surface. The lateral resolution of KFM is below 100 nm and the voltage resolution below 50 mV [83].

5.4 Surface treatment

Surface treatment was an important step in a sample fabrication process and for optimisation of OTFTs operation. Several objectives were achieved by treating a substrate surface: changing the surface wetting properties, surface cleaning and promoting the adhesion between a substrate and applied material.

5.4.1 Surface wetting properties

We analysed the surface wetting properties by measuring the contact angle between the deionized water and the SiO_2 surface (Fig. 5.9 (a)) before and after the SiO_2 surface was treated with various chemicals (Fig. 5.10). For this purpose, the contact angle meter CAM 100 (KSV Instrument), was used. The measurements were performed in Material research laboratory (University of Nova Gorica).



Figure 5.9: (a) Optical microscopy image of a deionized water drop on an untreated SiO₂ surface. The top part of the image shows a syringe with a narrow aperture containing the deionized water. Water is pushed through the syringe aperture until a contact is made between the water drop and the surface. At that point, contact angle between the surface and the water drop is formed, showing the wetting properties of the surface. (b) 4 x 4 μ m AFM image of an untreated SiO₂ surface.

We investigated wetting properties of SiO₂: prior to a surface treatment, after cleaning the surface with ammonia (NH₃) and after cleaning the surface with O₂ plasma. Measurements showed a significant change in the wetting properties of SiO₂ after both treatments. The initial contact angle value 43° of untreated SiO₂ decreased to 19° and 20° for NH₃ and O₂ plasma treatment (Fig. 5.10 (a-c)), respectively, indicating that the surface of SiO₂ became highly hydrophilic. Despite change in wetting properties, AFM investigation showed no drastic change in surface roughness of untreated SiO₂ (Fig. 5.9 (b)) compared to treated surfaces. The roughness of untreated SiO₂ was ~ 0.2 nm, which was unchanged after NH₃ and was slightly higher (~ 0.3 nm) after O₂ plasma treatment.



Figure 5.10: Optical microscopy image of (a) deionized water drop on untreated SiO_2 surface, (b) SiO_2 treated with NH_3 , (c) SiO_2 treated with O_2 plasma and (d) SiO_2 treated with Hexamethyldisilazane (HMDS).

5.4.2 HMDS surface treatment

Hexamethyldisilazane (HMDS) is a molecule often used for treating the SiO_2 surfaces in order to improve the performance of OTFT devices [84–86]. The advantages of HMDS are: stability in moisture, high purity, and simple method of deposition.

After HMDS is applied to a SiO₂ covered substrate, it reacts with SiO₂ (Fig. 5.11 (a)) forming a monolayer on the top of a SiO₂ layer. The resulting self-assembled monolayer (SAM) changes the OH-terminated SiO₂ to a CH₃-terminated as indicated in Fig. 5.11 (b). Our measurements showed, that HMDS treatment changed the wetting properties of SiO₂ substantially, resulting in a hydrophobic surface. The value of contact angle measured on HMDS treated SiO₂ increased to ~ 70° (Fig. 5.10 (d)).

SURFACE TREATMENT

We can apply HMDS on the SiO₂ surface from vapour phase, by spincoating or by deep-coating. Our results showed that the method of deposition didn't affect the final wetting properties of SiO₂ markedly, provided, that the substrates were heated before HMDS deposition. Values of contact angles were ~ 70° in all cases. However, on non-heated substrates the largest contact angle was measured on samples prepared by spin-coating method ~ 65° and the lowest on samples prepared by deep-coating technique ~ 52°. We also investigated the influence of HMDS treatment on surface roughness. AFM investigation showed no change in surface roughness between clean SiO₂ and HMDS-treated surface. In both cases, surface roughness remained ~ 0.2 nm.



Figure 5.11: Chemical reaction between SiO_2 and HMDS [87] (a). Resulting HMDS at the top of the SiO_2 surface (b).

The influence of HMDS treatment on the morphology of pentacene layers was also investigated. We compared the sub-monolayer thick pentacene layer deposited on clean (Fig. 5.12 (a)) and HMDS-treated SiO₂ surface (Fig. 5.12 (b)). The resulting grain density was substantially smaller for pentacene grown on an untreated SiO₂ surface. We interpret this result in terms of hydrophilicity of SiO₂ surface that promotes interaction between the incoming molecules and the existing islands, over the molecule-substrate interaction.



Figure 5.12: 4 x 4 μ m AFM images of sub-monolayer thick pentacene layer, deposited at substrate temperature T_s = 25°C and at deposition rate of 1 nm/min on untreated SiO₂ (a) and on HMDS-treated SiO₂ (b).

6 Microlithography

Microlithography indicates a method of lithography that is applied to integrated circuit fabrication. Rapid development of microlithography started in the early 1970s and it began with the optical lithography, where the etching tool was light with the wavelength between 300 nm and 450 nm. Over the time, the size of electronic devices decreased and thus also the wave length, therefore, deep UV light was introduced into the fabrication process with the wavelength ~ 250 nm and later even soft x-ray light with the wavelength ~ 1 nm. Since x-ray lithography requires more expensive equipment (e.g. synchrotron beam) UV light in combination with specially prepared phase-shifting masks is prefered by the major computer companies. Another approach of interdigitated circuits fabrication is electron beam lithography, where instead of light, electron beam is used for pattering. The methods is suitable for creating extremely fine structures, but due to the experimental set-up, it is moistly used for laboratory preparation of interdigitated circuits [88].

The channel size of transistors used in our experiment varied between 2 μ m and 5 μ m, therefore some form of advanced lithographic process had to be implemented for contact fabrication. We employed two methods of contact fabrication in our work: optical lithography and electron beam lithography. The basic procedure for both types of lithographic processes are schematically presented in Fig. 6.1 and involves modification of photoresist by: UV light/electron beam, developer, and remover, in order to obtain source-drain metallic contacts. Each step presented in Fig. 6.1 and components used in lithographic process, will be presented in continuation of this section.

The source-drain contact fabrication process was performed in its entirety at the National Laboratory TASC, Trieste, Italy. Preparation of the samples using optical lithography included the use of MJB3 mask aligner (Karl Suss), while sample preparation using electron beam lithography was performed using a customised electron microscope, (Carl Zeiss SMT Inc.). Metallisation of our samples was performed by evaporation of metal inside the vacuum chamber with a base pressure $\sim 10^{-4}$ Pa.

MICROLITHOGRAPHY



Figure 6.1: Schematic representation of the optical lithography procedure used for fabrication of source and drain contacts in a OTFT. (a) cleaning a substrate surface, (b) deposition of photoresist on top of the substrate, (c) exposure of a photoresist with UV light through the chromium mask, (d) development of a photoresist, (e) deposition of a metal on top of the substrate, (f) removal of the residual photoresist by immersing the samples into hot acetone or remover (LIFT-OFF process), (g) removal of an excess metal from the contacts edges by scrubbing.

6.1 Fabrication of chromium mask

The first step in lithographic process was fabrication of chromium mask. The mask was fabricated in accordance to our specifications by Delta Mask V.O.F., Holland. Delta Mask uses chrome blanks, fabricated by Hoya, Japan. Plates are made from the soda lime glass (the main chemical components of soda lime are: Ca(OH)₂ (~ 75%), H₂O (~ 20%), NaOH (~ 3%) and KOH (~ 1%), covered by a 98 nm thick chromium layer. The structures on the mask are fabricated by covering the plates with photoresist and pattering the desired feature with a laser. The excess photoresist is removed, determining the patterns for the chromium etch [89]. An example of chromium mask used

PHOTORESIST

in our work is presented in Fig. 6.2.



Figure 6.2: One of the chromium masks used for fabrication of source and drain contacts. It contains 44 source-drain contact templates, with different channel length ranging between 5 μ m and 25 μ m.

Critical parameters, defining the quality of the mask are: the accuracy of the pattern position, feature size control and defect density, which can be defined as extra or missing chromium film, resulting in incorrect pattern shape. In or case, the defect density was 0.1 defects/cm² and approximation of curves to 0.1 μ m, which was adequate for our application, since the channel lengths of source-drain contacts in our work ranged between 2 μ m and 25 μ m.

6.2 Photoresist

Photoresist is a chemical compound sensitive to UV light or to electron beam. While the chemical structure of photoresists is different, depending on the exposing media (soft UV light, deep UV light or electrons), the basic idea of photoresists response to the exposing media is similar.

6.2.1 Photoresist and its sensitivity to soft UV light

Photoresists can be divided in positive and negative tone photoresists. The classification depends upon the response of a photoresist to an exposing media. The positive tone photoresist becomes more soluble in a developer and negative tone photoresist becomes less soluble in a developer after the exposition.

The majority of our samples was fabricated by employing Microposit S1813 positive tone photoresist in a lithographic process. S1813 is sensitive to light of wavelength ranging between 350 nm and 450 nm [90]. Although the exact composition of S1813 is a matter of a trademark protection, we assume that the principal components of this photoresist are novolak resin and diazonaphthoquinone sensitizer (DNQ system) [88, 91]. The basic forms for the novolak resin and sensitizer are of the form shown in Fig. 6.3 [88].



Figure 6.3: Schematic representation of (a) a DQ sensitizer and (b) a novolak resin used in DNQ type of photoresists.

The novolak resin behaves as an inert aqueous-base soluble matrix polymer. Its dissolution rate is relatively high without the presence of DQ sensitizer. The function of DQ sensitizer is in lowering the dissolution rate in dark and promoting the dissolution rate in the presence of soft UV light (Fig. 6.4 (b)). High dissolution rate after exposing the DNQ system to the soft UV light is a result of the photochemical reaction in the sensitizer, transforming the DNQ system into base-soluble product (Fig. 6.4 (a)) [88].

6.2.2 Operational consideration

When a photoresist is exposed to UV light, active ingredients in the photoresist undergo a chemical reaction. Other components mixed in a photoresist may also absorb the UV light, but do not chemically react. The intensity of



Figure 6.4: (a) Representation of photolytic reaction of DQ sensitizer. (b) Dissolution rate of novolak resin free of DQ sensitizer, mixed with a DQ sensitizer and upon exposure to UV light.

UV light I, passing in the z direction through a photoresist reduces according to Lambert's law:

$$\frac{dI}{dz} = -\alpha I(z),\tag{6.1}$$

where α is the absorption coefficient of the material. Integrating eq. (6.1) for a homogeneous medium leads to:

$$I(z) = I_0 exp(-\alpha z), \tag{6.2}$$

where I_0 is the intensity of the light at z = 0. The absorption of light is caused by the presence of absorbing molecules, which concentration is denoted by cand the absorbing coefficient is denoted by a, therefore, α can be expressed as:

$$\alpha = a \cdot c. \tag{6.3}$$

In the case of photoresists, the absorption coefficient α changes during the exposition, because the photochemical reaction reduces the concentration of photoactive compound, therefore α must be written in the form:

$$\alpha = a_{PAC}c + a_p(c_0 - c) + \sum a_R c_R,$$
(6.4)

where a_{PAC} is the molar absorption coefficient of the photoactive compound, a_p is the molar absorption coefficient for the material that results from the photochemical reaction of the photoactive compound and the a_R are the molar absorption coefficients for all other compounds present in the photoresist and are assumed to be unchanged upon exposure to light. The initial concentration of the photoactive compound is represented by c_0 , and c_R represents the concentrations of all other constituents. Eq. (6.4) can be rewritten in the form of:

$$\alpha = A \cdot M + B, \tag{6.5}$$

where

$$A = (a_{PAC} - a_P)c_0$$

$$B = \sum_{R} a_R c_R + a_P c_0$$

$$M = c/c_0$$

For unexposed photoresist, M = 1, while for completely bleached photoresist M = 0. A represents the optical absorption that changes with exposure and B represents the components of the photoresist that do not change their absorption characteristic after the exposition. Values for A and B are measured and can be found in dedicated tables [88].

Once a film of a photoresist is exposed to light, the absorption is not uniform through the film. Parts of the photoresist, closer to the surface receive higher dosage, than those near the bottom. The calculation of photoresist exposure with depth and in time (M(t, z)) is a difficult task and can be done only with a computer, none the less, calculating M is a crucial step, since it is the only way of obtaining the photoresist profiles after the exposed part of photoresist is developed [88].

The composition of photoresists sensitive to electron beam, e.g. PMMA, SU-9 etc., is different compared to photoresists sensitive to soft UV light, but the basic idea of operation is the same in both cases. More information regarding photoresists sensitive to an electron beam can be found in the text written by P. R. Choudhury *et al.* [88].

6.3 Single layer optical lithography

The easiest method of optical lithography is a single-layer optical lithography. The term "single layer" indicates, that only one layer of photoresist is employed in the lithographic process. One of the most commonly used photoresists is Microposit S1813 positive tone photoresist.

We have applied photoresist on top of SiO₂ surface by the spin-coating technique. The rotational speed usually ranged between 3000 RPM and 4000 RPM. These rotational speeds assured uniform film thickness across the sample in the range of ~ 1.3 μ m, examined by the profilometer. The
measured film thickness corresponded to the thickness from the data sheets [90]. After the deposition of a photoresist the samples were heated at the temperature ranging between 90°C and 115°C for a time period between 90 s and 180 s, to remove the excess solvent from a photoresist. The samples were then put in a mask-aligner that is used to place the microlithographic mask in the physical contact with a sample. The samples were illuminated by a soft UV light through the chromium mask. The exposition time depended on the power of a UV light and ranged between 10 s and 20 s.



Figure 6.5: Schematic representation of photoresist profiles (a) after exposition and development for accurate exposition dose, (b) for underexposed photoresist and (c) for overexposed photoresist.

In order for a photoresist to receive a precise dose of UV radiation, the UV bulb had to be stable through the whole exposure. Precise determination of the photon flux was especially significant, when the channel length of interdigitated transistor legs downscale to ~ 5 μ m. If the photon flux was to small, the part of photoresist close to the SiO₂ surface received insufficient flux (the photochemical reaction between DQ sensitizer and UV light was not finished). When such samples were put in developer, the part of photoresist close to SiO₂ surface was not removed (Fig. 6.5 (b)). On the contrary, if the received photon flux was to high, it reached even the part of photoresist film, which was hidden under chromium mask, due to the light diffraction. When these samples were afterwards developed, all features representing the interdigitated transistor legs, were removed from the SiO₂ surface (Fig. 6.5 (c)).

The photoresist profiles in reality are not perpendicular to the substrate surface as shown in schematic representation in Fig. 6.5 (a), but are rather inclined, so that the separation between neighbouring sidewalls is smaller closer to the SiO₂ surface. This fact was confirmed by imaging several of our samples by the electron microscope. Some reports suggest that inclination of the sidewalls can be reduced, by soaking the sample covered with photoresist in chlorobenzene or toluene, and thereby modifying the top surface of the photoresist, so it is developed at a slower rate than the underlying resist [92, 93]. However, our results didn't confirm that. Even after soaking the sample with chlorobenzene, photoresist sidewalls were not perpendicular to the substrate surface (Fig. 6.6).



Figure 6.6: Electron microscope image of a sample soaked in chlorobenzene for 5 min prior to the development. The separation between sidewalls is $\sim 2 \ \mu m$.

After the photoresist was developed, the samples were inserted into vacuum chamber, where the evaporation of metal was performed. As discussed in section 4.3.3, the metal used for fabrications of source-drain metallic contacts must be appropriate in order to minimise the energy barrier at source/OS/drain interfaces. Suitable material for our application was Au. However, the adhesion between Au and SiO₂ is very poor, therefore additional thin layer (~ 20 Å) of Ti was deposited prior to Au evaporation. The metal evaporation was performed in the background pressure ~ 10^{-4} Pa.



Figure 6.7: Schematic representation of photoresist profiles after exposition, development and Au deposition. Because of the inclined sidewalls, the Au is deposited also on top of the photoresist sidewalls.

After the metal deposition, the excess photoresist was removed from the samples, by the LIFT-OFF process, which involved immersing the samples into hot acetone. At this point, problems involving inclined photoresist sidewalls, emerged. During the Au deposition the sidewalls of photoresist were covered with Au, render impossible for acetone to dissolve the excess photoresist (Fig. 6.7). Therefore, the combination of mechanical scrub and soaking the sample in acetone was needed to complete the LIFT-OFF process. But very often even the mechanical scrub didn't remove all Au from the transistor channel, resulting in fusion between the source and drain contacts (Fig. 6.8; top-right image, indicated with black ellipse). In addition, excess Au material very often remained at the edges of source-drain contacts (Fig. 6.8; top image, indicated with red ellipse).



Figure 6.8: Top-left image represents a sample at the end of lithographic process. The image shows, that Au was not completely removed in between transistor legs (indicated with black ellipse) and that the excess Au material was found at the edges of source-drain contacts (indicated with red ellipse). Top-right image show an AFM image of transistor legs. Part indicated with red square is additionally magnified and clearly shows rough edges found on source-drain contacts. Height profile show that the elevation at the borders of contacts can be four times higher, than the actual thickness of contacts.

6.4 Double layer optical lithography

In order to surpass some problems, presented in the previous chapter, we introduced the more advanced method of source-drain sample preparation so-called double layer optical lithography. The term "double layer" indicates, that two components are employed in lithographic process. One component was Microposit S1813 positive tone photoresist, and the other component was non-photosensitive material Microposit LOL1000, which dissolves in a photoresist developer in a controlled way [92].

First, LOL1000 was deposited on top of SiO₂ surface by the spin-coating technique. Because of poor adhesion of LOL1000 to SiO₂, additional treatment of SiO₂ was required prior to LOL1000 deposition. We treated SiO₂ surface either by mixture of H₂O₂ and H₂SO₄ (piranha solution) or by NH₃. Both treatments resulted in changing the wetting properties of SiO₂ as explained in section 5.4 and promoting the adhesion between LOL1000 and SiO₂. The rotational speed used for LOL1000 deposition was ~ 2000 RPM. At this speed, a uniform resist film was deposited on SiO₂ surface, with a thickness of ~ 100 nm, as measured by a profilometer and an AFM. The measured thickness agreed to the thickness from the data sheets [94]. After LOL1000 deposition, the samples were baked at the temperature 170° C for 10 min to remove the excess solvent from the resist. The second step was deposition of S1813 on top of LOL1000. The deposition of S1813 followed the same steps described in section (6.3).



Figure 6.9: Electron microscope image of a photoresist profiles fabricated by the double layer lithography involving SPR500-A photoresist and LOL1000. Circles on the image indicate the undercut in the photoresist sidewalls. The image was taken from the reference [94].

After LOL1000 and S1813 deposition, the samples were exposed to UV light through the chromium mask. The next step was removal of S1813

layer in a dedicated developer. After removing S1813, soluble LOL1000 was reached by the developer. If the illumination and developing time were accurate, only parts of LOL1000 beneath the removed S1813 were dissolved, forming the undercut presented in Fig. 6.9 [94].

After development, we placed samples into vacuum chamber, where Au was evaporated. The final step was removing the excess LOL1000, S1813 and Au, by immersing the sample into dedicated remover. At this point the benefit of double layer lithography become evident. Since the undercut is present in photoresist profiles, Au is not deposited over the photoresist sidewalls (Fig. 6.10), enabling the remover to dissolve the photoresist and remove the excess Au easily. In this way well defined metal patterns are achieved (Fig. 6.11). The drawback of double layer optical lithography is that the method is even more susceptible to the oscillation in received photon flux and thus the UV bulb must be even more stable.



Figure 6.10: Schematic representation of photoresist profiles after exposition, development and Au deposition. Since the undercut is present, Au is not deposited on top of photoresist sidewalls.



Figure 6.11: Source-drain metallic contacts fabricated by double layer optical lithography. Right image shows a complete sample, where large pads are used for connecting the active part of transistor structure (indicated with red circle) with a measuring equipment. The active part is magnified in left-bottom image, showing the interdigitated transistor legs. Magnification of these legs (top-left image) shows, that the transistor channels are clear of Au.

6.5 Single layer electron-beam lithography

Electron-beam lithography was introduced in our source-drain contact fabrication process, to overcome the problems involving the stability of UV light, described in previous two sections. The drawback of electron beam lithography is a relatively small area that can be exposed to an electron beam. The limiting size in our case was 500 x 500 μ m, therefore, two steps lithography had to be employed. In the first step, larger pads, used to connect the transistor device with the measuring equipment, were fabricated by using the double layer optical lithography described in section 6.4. Since the separations between large pads were ~ 275 μ m, issues regarding stability of UV light were not significant. After large pads were finished, the electron-beam lithography was employed to fabricate the small interdigitated transistor legs, with the channel length ~ 5 μ m.

Photoresist used in our work was polymethylmethacrylate (PMMA). The rotational speed used for deposition was ~ 3000 RPM. At this speed, uniform films of PMMA photoresist were deposited on SiO₂ surfaces, with a thickness of ~ 400 nm measured by the profilometer. The adhesion between PMMA and SiO₂ was very strong, so additional surface treatment prior to deposition was not required. After deposition of PMMA, the samples were baked at the temperature of 170°C for 10 min and mounted into the electron microscope vacuum chamber, where the photoresist exposition by the electron beam was performed. The resulting photoresist profiles were perpendicular to the surface (Fig. 6.5 (a)), which is an important advantage of the method. After development, the samples were placed inside the vacuum chamber, where Au and Ti were deposited. The final step was removing the excess photoresist by the LIFT-OFF process. PMMA was not completely removed from the surface by the LIFT-OFF process, therefore, additional cleaning of surface by O₂ plasma was required.

Another advantage of the electron-beam lithography was the requirement of only one sample for determining the exposition dose and the development time for the photoresist. It was done by fixing the development time and increasing the exposition dose (Fig. 6.12). The exposition dose of electron beam in Fig. 6.12 increased from the left part of the sample to the right. The photoresist on the left side was underexposed. Consequently, it was not completely removed by development, and as a result Au was not removed by the LIFT-OFF process. On the contrary, the right part of the sample was overexposed. The effect can be slightly seen in the corner marked with the circle (Fig. 6.12). Instead of sharp, 90° corners, overexposed parts show slightly round shaped features (the effect can be better observed by looking the sample directly through the optical microscope). After the right exposi-



tion dose was found, almost all samples were fabricated without defects.

Figure 6.12: Electron microscope image of a sample fabricated by the combination of double-layer optical lithography (large pads) and single-layer electron-beam lithography (small transistor legs, placed between the large pads).

7 Evolution of source-drain current as a function of pentacene layer thickness: influence of Ti adhesion layer

We have investigated the influence of Ti adhesion layer on charge transport properties of pentacene-based organic thin film transistors (OTFTs). The Au source-drain contacts were prepared by using 3 nm-thick, 2 nm-thick, and controlled samples without Ti adhesion layer. The OTFTs were investigated in situ, during the evaporation of pentacene layers by measuring the sourcedrain current (I_{sd}) as the thickness of pentacene layer progresses. We have associated the delayed onset of I_{sd} , observed in current vs. thickness curves, for the OTFTs fabricated with the thick Ti adhesion layers, with the high hole injection barrier at Ti/pentacene interface. The onset of I_{sd} in these OTFTs was observed only after the nominal thickness of pentacene layers was comparable with the thickness of Ti adhesion layers.

7.1 Introduction

Organic thin film transistors (OTFTs) have attracted much attention due to their possible applications in organic electronics. The geometry frequently used in fabrication of OTFTs is bottom-contact bottom-gate transistor geometry (BC) [1, 48].

Experiments show that the critical factor determining the performance of BC OTFTs is the resistance at source/organic semiconductor (OS) and OS/drain interfaces. The origin of contact resistance in the BC OTFTs is ascribed to the defects in the semiconductor layer in the vicinity of source and drain electrical contacts, and to the hole injection barrier (φ) at the metal-contacts/OS interfaces [8, 50, 51].

Source and drain contacts in the pentacene-based OTFTs are usually comprised from several nm-thick Ti adhesion layer, covered by 30 nm to 50 nm-thick Au layer. Although, the metal/organic interfaces do not follow the Scottky-Mott model, we can use the model to estimate the φ at the pentacene/Au interface (φ_{Au}) and at the pentacene/Ti interface (φ_{Ti}). By using the data from Refs. [95, 96], we estimated $\varphi_{Au} \sim 0.1$ eV and $\varphi_{Ti} \sim 0.9$ eV. Results indicate that the charge carrier injection from Ti into the pentacene is limited due to a high φ_{Ti} . The supposition was confirmed in the experiment performed by Yoneya *et al.* [97].

Since the φ_{Ti} is high, we need to know if the sidewalls of Ti layer beneath the Au are exposed to form the contact with pentacene, and therefore influence to the charge transport in OTFTs. We expect that the effect of Ti would be even more pronounced, if the thickness of transport layer in pentacene is comparable with the thickness of Ti adhesion layer.

One approach to determine the thickness of the transport layer in OSs was by fabricating a series of devices with various OS layer thicknesses and following the evolution of current/mobility as the OS layer thickness progresses [98]. In this work we used an alternative method via in situ electrical characterisation of OTFTs during the evaporation of the OS layer. By comparing the evolution of the source-drain current as a function of the pentacene layer thickness with that of the pentacene layer morphology, we were able to determine the thickness of transport layer in pentacene. Similar approach was also taken by Muck *et al.* [52] on DH4T and by Kiguchi *et al.* [99] on pentacene. By observing the delayed onset of current in current vs. thickness curves for samples prepared with various thicknesses of Ti adhesion layer, we determined a critical thickness of Ti adhesion layer, below which the influence to the charge transport in OTFTs is negligible.

7.2 Experimental methods

We have used the bottom-gate, bottom-contact geometry of OTFTs in our experiment. Heavily doped p-type silicon wafer, covered by thermally-grown, 200 nm-thick SiO₂ was used as a substrate. Drain and source metallic contacts were fabricated by optical and electron-beam lithography, and thermal evaporation. The contacts comprised 2 nm to 3 nm-thick Ti adhesion layer, covered by 30 nm to 50 nm-thick Au layer. Control samples without Ti adhesion layer were also fabricated. OTFTs channel lengths ranged between 4 μ m and 5 μ m and the channel widths ranged between 0.3 mm and 2.3 mm.

Pentacene used in our experiment was purchased from Aldrich Chemical Co., and was not additionally purified. Pentacene was evaporated in a vacuum chamber, with the background pressure of $5 \cdot 10^{-6}$ Pa. The deposition rate ranged from 0.5 nm/min to 1.5 nm/min, and the substrate temperature ranged between 25°C and 65°C. Source, drain and gate contacts were connected with a power supply (Keithley 617 or Keithley 6487) and an ampere meter (Keithley 2400) via an electrical vacuum feedthrough. The power supply was connected with the gate electrode to control the gate voltage applied to the transistor, and the ampere meter was used to measure the current through the transistor, and to supply a source-drain voltage. The measurement was initiated when the mechanical shutter blocking the sample surface off the pentacene molecules was removed. When sufficient amount of material was deposited onto the substrate, the current through the transistor started to increase. We performed several successive source-drain current-voltage (I-V) measurements on a single transistor in situ during the evaporation of pentacene layer. We were therefore able to follow the evolution of I-V characteristics as a function of pentacene layer thickness. The voltage applied to gate contact during an I-V sweep was -15 V, and the source-drain voltage ranged between +5 and -20 V.

In order to investigate the correlation between the source and drain current (I_{sd}) and the pentacene layer thickness, we prepared several samples with different pentacene layer thicknesses deposited at the identical growth conditions (the deposition rate 1.5 nm/min and the substrate temperature 65°C) and investigated the morphology by AFM operating in air.

7.3 Results and discussion

Fig. 7.1 (a) shows a I_{sd} as a function of pentacene layer thickness. The values of I_{sd} were extracted from the I-V curves in the saturation regime at $V_{sd} = -25$ V and $V_g = -15$ V. Examples of I-V characteristics for constant

 $V_g = -15$ V and for pentacene layer thicknesses 1.6 nm, 10 nm, and 50 nm are presented in Fig. 7.1 (b).



Figure 7.1: (a) evolution of I_{sd} as a function of pentacene layer thickness for BC OTFT with 2 nm-thick Ti adhesion layer. Pentacene deposition conditions were: deposition rate 1.5 nm/min and the substrate temperature 65°C. Presented values of I_{sd} were obtained in saturation regime of device operation at $V_{sd} = -25$ V and $V_g = -15$ V. (b) I-V characterisation during the pentacene layer deposition at constant $V_g = -15$ V and alternating V_{sd} between 0 V and -25 V, by the 5 V step, for the layer thicknesses: 1.6 nm, 10 nm and 50 nm from the top to bottom measurements, respectively.

From Fig. 7.1 (a) we see an abrupt increase of I_{sd} in the beginning stages of layer growth, followed by the saturation of I_{sd} for the thicker layers. Similar behaviour was observed also by Kiguchi et al. [99] on pentacene-based OTFTs. They observed an increase in I_{sd} which started at nominal layer thickness 1 nm and persisted up to the thickness \sim 9 nm, above which the plateau in I_{sd} was observed. The experiment, performed by Muck *et al.* [52] on dihexylquaterthiophene (DH4T), showed a more complex evolution of the field-effect mobility in OTFTs as a function of the DH4T layer thickness. For the small coverages below a certain threshold thickness no significant I_{sd} was observed. Only after approximately 0.54 monolayer thickness was reached, I_{sd} through OTFTs was observed. The maximal value of the field-effect mobility was reached upon completion of the first layer, after which, a significant decrease in the field-effect mobility was observed, which was attributed to the increasing density of second monolayer island boundaries during growth. These second layer boundaries are expected to disturb the mobile charges in the first layer below. Second maximum of field-effect mobility was reached after the completion of the second layer. Further deposition led to a decrease in the field-effect mobility and was not recovered upon the completion of the third or the subsequent layers. Monotonic decrease in the field-effect mobility for higher coverages was attributed to the higher contact resistance, which was explained by the lateral diffusion of DH4T towards the contacts, which depleted the neighbouring areas in channel along the contact line.

The thickness of accumulation layer (L_a) in OSs can be estimated by applying:

$$L_a = \frac{2\epsilon_S kT}{qC_i V_q},\tag{7.1}$$

which is derived by solving the Poisson's equation [26]. By estimating $\epsilon_S = 3\epsilon_0$, where ϵ_0 is the permittivity of free space, k is the Boltzmann constant, T = 300 K, $C_i \sim 10^{-8}$ F/cm² and $|V_g| = 10$ V, L_a is estimated to ~ 1 nm, which is in the most OSs less than a monolayer thickness. Although the physical size of the transport layer doesn't necessary coincide with the accumulation layer [98], the above result implies that the mobile charge carriers in the OS layers are concentrated close to the OS/insulator interface.

More meticulously is I_{sd} evolution as a function of pentacene layer thickness presented in Fig. 7.2. Immediately after the growth was initiated, we observe no I_{sd} between the source and drain contacts. This situation persists until a sharp increase in I_{sd} is observed at the nominal layer thickness 1.6 ± 0.2 nm. Within ~ 4 nm of pentacene layer thickness the increase of I_{sd} becomes slower and almost completely saturates at the nominal layer thickness 10 nm.



Figure 7.2: Evolution of I_{sd} as a function of pentacene layer thickness for BC OTFT with 2 nm-thick Ti adhesion layer. Pentacene deposition conditions were: deposition rate 1.5 nm/min and the substrate temperature 65°C. Presented values of I_{sd} were obtained in saturation regime of device operation at $V_{sd} = -25$ V and $V_q = -15$ V.

The AFM images presented in Fig. 7.3 correspond to the nominal pentacene layer thicknesses (NT) of 1 nm (a), 2 nm (b), 3 nm (c), 5 nm (d), 7 nm (e), and 50 nm (f). Pentacene layer morphology at NT 1 nm is characterised by monolayer islands (Fig. 7.3 (a)). The darker parts in Fig. 7.3 (a) represent the SiO_2 insulator, free of pentacene material, and the bright areas represent the pentacene islands forming on the surface. At NT 2 nm the islands have coalesced, but voids inside the first layer are still present (Fig. 7.3 (b); indicated with green arrows). The brighter areas in Fig. 7.3 (b) (indicated with black arrows) show the successive pentacene layers, indicating a 3D island growth after the formation of the first layer. The first layer was completed at the latest at NT 3 nm (Fig. 7.3 (c)). At that point, the coverage of second layer was $\sim 45\%$ and the islands in the second layer were not jet connected to form a continuous layer. Morphological investigation at NT 5 nm showed that the coverage of the second layer increased to ~ 80 %. Despite a relatively large coverage numerous voids between the second layer islands were observed (Fig. 7.3 (d), indicated with green arrows). These voids were almost completely closed at NT 7 nm (Fig. 7.3 (e)). Based on the layer morphology observed in Fig. 7.3 (e), we estimated the coverage of the second layer at NT 7 nm to $\sim 90\%$.



Figure 7.3: Atomic force micrographs of pentacene layers deposited on SiO₂. The scan size is $7x7 \ \mu m$. Nominal thicknesses of pentacene layers are 1 nm (a), 2 nm (b), 3 nm (c), 5 nm (d), 7 nm (e) and 50 nm (f). Pentacene deposition conditions were: deposition rate 1.5 nm/min and substrate temperature 65° C.

66EVOLUTION OF SOURCE-DRAIN CURRENT AS A FUNCTION OF PENTACENE LAYER TH

The evolution of I_{sd} (Fig. 7.2) can be explained, based on the morphological measurements presented in Fig. 7.3. The onset of I_{sd} current was observed for the NT ~ 1.6 , at which point, the pentacene island coalesced and thus connecting the pathway for electric charge between the source and drain electrodes. The increase of I_{sd} up to the NT ~ 3 nm was explained by filling the voids between the pentacene islands and forming the continuous first layer. Morphological investigation of thicker layer showed that the second-layer islands did not coalesce until the NT was ~ 7 nm, therefore, I_{sd} increase for the layer thickness between 3 nm and 7 nm can't be attributed to the formation of additional pathways in the second layer, therefore, observed increase of I_{sd} must be explained, by the second layer providing additional paths for the carriers generated in the first layer, by bridging across the grain boundaries of the first layer [98]. We note, that this behaviour of I_{sd} observed in pentacene, differs from the behaviour reported by Muck et al. [52] for DH4T, where the second layer disturbed the mobile charges in the first layer. Morphological investigation showed, that the contribution of charge transport across the second layer was possible only after the NT > 7 nm, when the sufficient coverage of the second layer was observed to form the pathways for electric charge between the source and drain electrodes. The I_{sd} was almost completely saturated at NT ~ 10 nm. Based on the morphological observation of pentacene layers and the evolution of I_{sd} we can conclude that the majority of mobile charge, and therefore the thickness of transport layer is limited inside the first-two monolayers.

Fig. 7.4 shows I_{sd} evolution as a function of pentacene layer thickness measured for samples, where source and drain contacts comprised 2 nmthick (Fig. 7.4; red circles) an 3 nm-thick (Fig. 7.4; blue triangles) Ti adhesion layer, covered by 50 nm-thick Au layer. Controlled samples without Ti adhesion layer were also fabricated (Fig. 7.4; black squares). When 3 nmthick Ti layer was employed in lithographic process (Fig. 7.4), the onset of current was observed at NT ~ 2.6 nm, which corresponds to the thickness of Ti adhesion layer. In contrast, when 2 nm-thick or samples without Ti adhesion layer were used, the onset of current was observed at NT 1.6±0.2 nm and is coupled to the coalescence of pentacene islands in the first layer, and thereby, forming the electrical pathways between source and drain electrodes.

We propose the following explanation for the delayed current onset observed in Fig. 7.4. Schematic representation of samples fabricated with the single layer optical lithography and employing ~ 3 nm-thick Ti layer is presented in Fig. 7.5. The injection barrier at the Ti/pentacene interface is relatively high, therefore, carrier injection from Ti into the pentacene was minimal. We therefore conclude, that the current flow through OTFTs was possible, only after the pentacene reached the Au layer (Fig. 7.5) at



Figure 7.4: Evolution of I_{sd} as a function of pentacene layer thickness for OTFT, where source-drain contacts were fabricated without Ti adhesion layer, with ~ 2 nm and ~ 3 nm thick adhesion layer, indicated with black, red and blue, respectively.

 $NT \sim 2.6$ nm (Fig. 7.4). Since the transport layer in pentacene is bounded inside the first-two pentacene monolayers, the majority of mobile charge car-



Figure 7.5: Schematic representation of source-drain metallic contacts fabricated with ~ 3 nm-thick Ti adhesion layer.

riers are spatially concentrated in the layer which is comparable with the thickness of Ti adhesion layer. Smaller I_{sd} observed for the samples fabricated using 3 nm-thick adhesion layer (Fig. 7.5) is therefore ascribed to the deteriorating influence of Ti adhesion layer to charge transport between source-drain contacts. Similar result was reported also by Yoneya *et al.* [97]. They measured an abrupt increase of the contact resistance in BC pentacene-based OTFTs, when the thickness of Ti was ~ 3 nm, which corresponds well to the critical thickness of Ti adhesion layer measured in our experiment.

7.4 Conclusion

We investigated the influence of Ti adhesion layer to the charge carrier transport in bottom-contact pentacene-based organic thin film transistors. In situ electrical measurements of source-drain electrical current as a function of pentacene layer thickness demonstrate that the majority of current is transported by the first two molecular layers of pentacene. In addition, we observe an onset of source-drain current that depends on the thickness of Ti layer. If the thickness of Ti layer exceeds the thickness of two pentacene layers, the onset of the current is delayed until the pentacene layer thickness exceeds two molecular layers. This result has important implications in the source-drain contact fabrication process, since a Ti layer must be employed to promote the adhesion between Au layer and SiO₂. Our results show that in order to avoid the influence of Ti adhesion layer on charge carrier transport in OTFTs, the thickness of Ti layer must not exceed 2 nm.

8 Morphology of the metal-organic semiconductor contacts: the role of substrate surface treatment

We have systematically investigated the role of SiO_2 surface treatment on pentacene morphology at the metal/pentacene interface. The substrates included as-grown SiO_2 and SiO_2 surface, treated by self-assembled monolayer (SAM) of hexamethyldislazane (HMDS). The resulting OTFTs were investigated in situ, during growth of pentacene layer by measurements of current-voltage characteristics, and ex situ by an atomic force microscopy. Our results show that the effective field-effect mobility of pentacene decreases with decreasing growth rate. In addition, for low growth rates, we observed an existence of discontinuous pentacene coverage at the metal-pentacene interface. We associate the decrease in mobility to this morphological feature. We have found that HMDS treatment results in a reduced areal density of extended structural defects. However, at the lowest growth rates even HMDS treatment can not promote wetting of the metallic contacts with pentacene in order to close the gap between pentacene and the metallic contact.

8.1 Introduction

An organic thin film transistors (OTFTs) based on pentacene are likely to become an important component in large-area electronic applications [1, 48], sensors [100, 101], and in organic displays [102, 103]. This is because high filed-effect mobility is achieved when pentacene is used in OTFTs applications. Typical OTFT includes thin organic semiconductor (OS) layer deposited between two metallic contacts on a suitable substrate. Great deal of the present OTFTs are fabricated by vacuum evaporation of pentacene on SiO₂-covered highly-doped Si substrates that act as a gate electrode.

Atomic force microscopy (AFM) imaging of vacuum evaporated pentacene layers on SiO₂ show polycrystalline nature of layers. The morphology of a completed pentacene layer is therefore characterised by grains whose shape and size depend on processing parameters such as deposition rate [10, 24] and substrate temperature [10, 24] and surface treatment of the insulator [11].

Assuming that grain boundaries are electrically active crystallographic defects that introduce trap levels into the energy structure of a pentacene layer, we would expect that hole mobility decreases with increasing density of grain boundaries. In other words, pentacene layers with larger islands are expected to exhibit larger field-effect mobility. This was confirmed experimentally by Horowitz [104], on the octithiophene (8T) based OTFTs and by Di Carlo *et al.* [9] who measured field-effect mobility in pentacene based OTFTs. In both cases the substrate was not treated with SAM prior to deposition of semiconductor active layer. On the other hand, when surface is treated with SAM, opposite trend is observed. Despite the reduced grain size which is the result of surface treatment, pentacene layers exhibit higher field-effect mobility [11, 38].

In addition to the morphological features of the pentacene layer, the performance of an OTFT is influenced by the microscopic interface environment at the interface between the pentacene layer and a source and drain metallic contact. The electronic parameters of the interface may give rise to an increased contact resistance. Therefore it is important to understand the relationship between the chemical/structural characteristics of the OS/metal interface and charge carrier transport in OTFT. For example the difference in mobility between the top-contact and bottom-contact OTFT was associated to the different morphology of the pentacene layer near the metallic contacts [50].

In this work we have investigated the influence of pentacene film morphology near the metallic contacts on electric charge transport in OTFTs. The morphology of pentacene layers was controlled by the flux of pentacene molecules. For lower growth rates we observe a region near the metal contact where no pentacene layers were observed. We associated this feature to lower "effective" field-effect mobility measured in our experiment. Additionally, we investigated the morphology of pentacene layers in the vicinity of the metallic contacts for treated and untreated substrates. We ascribed the difference in morphology to the treatment of SiO₂ surface with HMDS.

8.2 Experimental methods

We have used the bottom-gate, bottom-contact geometry of OTFTs in our experiment. Heavily doped p-type silicon wafer, covered by thermally-grown, $200 \text{ nm-thick SiO}_2$ was used as a substrate. Drain and source metallic contacts were fabricated by thermal evaporation and optical lithography. The contacts comprised 2 nm-thick Ti adhesion layer, covered by 50 nm-thick Au layer. The device channel length was $l = 5 \ \mu m$ and the channel width was W = 2.3 mm. To improve the performance of OTFT we treated the surface of several samples with HMDS, before depositing pentacene active layer. In order to observe the influence of the surface treatment to the morphology of pentacene layers in the vicinity of metallic contacts, some sample remained untreated. Pentacene used in our experiment was commercially purchased from Aldrich Chemical Co. and was not additionally purified. The pentacene was evaporated in a high-vacuum chamber, with the base pressure of $5 \cdot 10^{-6}$ Pa. The deposition rate ranged from 0.05 nm/min up to 1.2 nm/min, and the substrate was at room temperature during organic thin film growth. The pentacene layer thickness ranged from nominally 2 nm to nominally 17 nm, and was determined in situ by quartz thickness monitor.

Source, drain and gate contacts were connected with a power supply (Keithley 617) and an ammeter (Keithley 2400) via an electrical vacuum feed-through. The power supply was connected with the gate electrode to control the gate voltage applied to the transistor and the ammeter was used to measure the current through the transistor and to supply source-drain voltage. The measurement was initiated when the mechanical shutter blocking the sample surface off the pentacene molecules was removed. When sufficient amount of material was deposited onto the substrate, the current through the transistor started to increase.

We performed several successive current-voltage (I-V) measurements on a single transistor in-situ during the evaporation of pentacene layer. We were therefore able to follow the evolution of I-V characteristics as a function of pentacene film thickness. The voltage applied to gate contact during an I-V sweep was -15 V, and the source-drain voltage ranged between +5 and -20 V. The time interval between successive sweeps varied. Its length depended on to the deposition rate and ranged between 1 and 8 s. In order to minimise the transistor stressing, the source-drain and the gate voltage was put to 0 V between successive sweeps. Experiments showed that extended transistor operation could result in a reduction of the source-drain current through the transistor [105] and in a shift of threshold voltage [106]. Since the threshold voltage was not measured during the experiment, we wanted to minimise the effect of transistor stressing by switching off the transistor between successive sweeps.

After the deposition of an active layer, the morphology was observed ex situ by an atomic force microscope (AFM) operating in air. In order to investigate in depth the eventual effects of microscopic interface environment on the performance of our OTFTs we focused our AFM investigations to the regions in close proximity of the metallic contacts of the source and drain.

8.3 Results and discussion

Fig. 8.1 (a) shows the effective field-effect mobility plotted in logarithmic scale. Different curves correspond to different growth rates used during pentacene evaporation, and correspond to nominal growth rates of 1.2 nm/min, 0.15 nm/min and 0.05 nm/min, from top to bottom, respectively. The effective field-effect mobility values were calculated from the I-V curves in the saturation regime, following the model frequently used to predict operation of inorganic transistors [25].

The curves presented in Fig. 8.1 (a), therefore describe the evolution of the charge carrier transport as a function of pentacene layer thickness between the source and drain contacts. Immediately after the onset of growth, we observe no charge carrier transport between the two contacts. This situation persists until a sharp increase in mobility is observed. Within 1-2 nm of pentacene layer thickness the increase in mobility becomes slower. We note that the maximum value obtained for mobility depends on the pentacene growth rate (Fig. 8.1 (a)). At the growth rate of 1.2 nm/min we have obtained a maximum value of hole mobility of $0.06 \text{ cm}^2/\text{Vs}$. Similar behaviour, decreasing field-effect mobility of pentacene based OTFT with decreasing growth rate, was reported by Park *et al.* [107]. The onset of charge carrier transport occurs at pentacene thickness of 1.3 ± 0.2 nm. The differences in the thickness, at which the onset of charge carrier transport occurs, between different growth rates, are within the experimental error of the thickness measurement.

Morphology of pentacene layers grown by vacuum evaporation on SiO_2 as



Figure 8.1: Evolution of an effective field-effect mobility as a function of pentacene layer thickness obtained in the samples fabricated by three different growth rate (1.2 nm/min, 0.15nm/min and 0.05 nm/min, top to bottom) (a). Evolution of an effective field-effect mobility as a function of thickness obtained in the sample fabricated by a growth rate of 0.05 nm/min (b).

a function of thickness was studied by Ruiz *et al.* [108]. Their results show that a second molecular layer starts to nucleate before a continuous first layer is formed. X-ray diffraction measurements of pentacene layers on SiO_2 indi-

cate that a single-layer thickness of pentacene amounts to 1.5 nm [109]. From a sharp increase of mobility at pentacene layer thickness of $1.3 \pm 0.2 \text{ nm}$, observed in our experiment (Fig. 8.1 (a)), we may therefore conclude that a connected current pathway between the source and the drain contact exists, even before a continuous pentacene layer is achieved. The formation of a continuous layer therefore proceeds by merging of the isolated islands. Such sharp and sudden increase in mobility before the formation of a continuous OS layer was reported also by Muck *et al.* [53], who performed similar experiment to ours but using dihexylquaterthiophene (DH4T) as an active organic layer in OTFTs.

From Fig. 8.1 (a) we see that the effective field-effect mobility vs. pentacene layer thickness in the samples fabricated by using the deposition rate 0.05 nm/min markedly differs from the mobility vs. pentacene layer thickness in the samples fabricated by using the deposition rate of 1.2 nm/min and 0.15 nm/min. The latter curves exhibit a monotonic increase in mobility as the pentacene layer thickness increases. The former, on the other hand, exhibits a marked plateau in the pentacene layer thickness range between 3 nm and 10 nm. This is more evident in Fig. 8.1 (b), where we show effective field-effect mobility as a function of pentacene layer thickness for the samples fabricated by using the deposition rate of 0.05 nm/min. In order to clarify this marked difference in electronic properties of the OTFTs fabricated by using different pentacene growth rates we have performed a systematic investigation of morphological parameters of pentacene layers in light of varying growth rate.

The relationship between the morphology of pentacene layers and the growth rate has been documented in Ref. [24]. In Fig. 8.2 we exemplify AFM scans of pentacene layers deposited on HMDS-treated SiO₂ using different growth rates. The scanned area shown is $4x4 \ \mu m^2$. The individual images correspond to the growth rates of 1.2 nm/min, 0.15 nm/min and 0.05 nm/min, Fig. 8.2 (a), (b) and (c), respectively. The thickness of the pentacene layers is 18 nm, 17 nm and 15 nm in Fig. 8.2 (a), (b) and (c), respectively. The thicknesses correspond to the maximum thicknesses used to determine mobility vs. thickness curves shown in Fig. 8.1. We see that the pentacene layer is characterised by grains, which size depends on the growth rate. For the growth rate of 1.2 nm/min the average grains size is 0.45 μ m, for growth rate of 0.15 nm/min the average grains size is 0.78 μ m, and for the growth rate of 0.05 nm/min the average grains size is 0.82 μ m. This is what we would expect based on the deposition-diffusion-aggregation (DDA) model [110]. Similar behaviour was also observed experimentally by Pratontep et al. [10] and is a signature of reduced surface mobility of the pentacene molecules as the flux of incoming molecules increases. A white region in Fig.



Figure 8.2: Atomic force micrographs of pentacene layer deposited on SiO₂ with three different deposition rates. The scan size is $4x4 \ \mu m^2$. (a) deposition rate 1.2 nm/min; (b) deposition rate 0.15 nm/min; (c) deposition rate 0.05 nm/min. Images were scanned in the vicinity of metallic source-drain contacts. The narrow white stripe indicates the metallic contact. Area in image (c) indicated by arrows shows a region near the metallic contact of width between 10 nm and 120 nm, where no pentacene islands are present.

8.2 (a), (b) and (c) corresponds to source metallic contact. We note that Fig. 8.2 (c) shows a region near the metallic contact of the width between 10 nm and 120 nm, where no pentacene islands are present (indicated by arrows). This indicates that low growth rates may result in a discontinuous pentacene film near the metallic contacts. To investigate further the evolution of morphology of pentacene layer near the metallic contacts we have examined pentacene layers of different thickness and show the results in Fig. 8.3.

76MORPHOLOGY OF THE METAL-ORGANIC SEMICONDUCTOR CONTACTS: THE ROLE OF



Figure 8.3: Atomic force micrographs of pentacene layer deposited on SiO_2 at a growth rate of 0.05 nm/min. The scan size is 4x4 μ m². The images correspond to pentacene layer thickness of 2 nm (a), 4.5 nm (b), and 10 nm (c). The white stripes in the images correspond to metallic contacts of the source. Isolated regions in image (a) where pentacene islands touch the metallic layer are indicated by black arrows and white arrows indicate a pentacene island that is in contact with metallic electrode but the islands are not connected to the layer inside the channel.

In Fig. 8.3 we show AFM scans of pentacene layers deposited on HMDStreated SiO₂. The scanned area shown is $4x4 \ \mu m^2$. The individual images correspond to pentacene layer thickness of 2 nm, 4.5 nm, and 10 nm, Fig. 8.3 (a), (b), and (c), respectively. Fig. 8.3 (a) shows the pentacene layer of thickness, at which the onset of mobility saturation was observed (Fig. 8.1 (b)). We see that a substantial portion of metallic contact is free of pentacene islands. Isolated regions where pentacene islands touch the metallic layer are indicated by black arrows. White arrow exemplifies a pentacene island that is in contact with metallic electrode, however its height exceeds average pentacene layer height inside the channel (2 molecular layers). In addition, these islands are not connected to the layer inside the channel. The width of the region that is not covered by pentacene may reach values as high as 350 nm. Uncovered regions of similar size are found also inside the channel. As the thickness of the pentacene layer increases to 4.5 nm, the exposed regions inside the channel become covered with pentacene islands. Near the metallic contacts however, relatively broad region of the substrate remains uncovered (Fig. 8.3 (b)). This surface condition persists also at thickness of 10 nm, as seen in Fig. 8.3 (c). It is apparent, though, that the amount of material is sufficient to partially cover the exposed regions.

The sequence of different pentacene layer thicknesses shown in Fig. 8.3 confirms a layer-plus-island growth mode of pentacene on HMDS-treated SiO_2 . In addition, in Fig. 8.3 (a) we see that the growth near the metallic contacts is predominantly three-dimensional, whereas inside the channel a layer-plus-island growth mode is retained. We note that the existence of a gap between the metallic contacts and DH4T layer in the initial stages of growth was observed also by Muck et al. [53]. We associate the absence of uncovered region in the samples fabricated with higher growth rates to a reduced surface mobility of the pentacene molecules. Due to an increased flux of incoming molecules nucleation of islands is favoured, regardless of the location on the substrate. Therefore, the morphology of the layer is characterised by relatively small islands throughout the channel (Fig. 8.3). At lower fluxes of incoming molecules the molecules already present on the surface have sufficient mobility to seek optimum positions. Vicinity of gold contacts represents an unfavourable environment for two-dimensional island formation, relative to the region far away from the contacts. The resulting morphology near the contacts is therefore characterised by uncovered regions or, at best, by isolated three-dimensional islands.

Electric charge transport across such interface is less efficient than in the case of homogeneous metal/pentacene interface. This is reflected by more than one order of magnitude lower hole mobility, observed in the samples fabricated by the growth rate of 0.05 nm/min (Fig. 8.1 (a), bottom-most curve). The existence of plateau in mobility vs. thickness curve (Fig. 8.1 (b)) is likely to be a consequence of gradual closing of the uncovered region near the metallic contacts exemplified in sequence of AFM images in Fig. 8.3.

In order to investigate the influence of HMDS surface treatment to the performance of OTFTs, an I-V characterisation during the deposition of pentacene active layer on several samples free of HMDS surface treatment

78MORPHOLOGY OF THE METAL-ORGANIC SEMICONDUCTOR CONTACTS: THE ROLE OF

was performed. We concentrate our efforts to low deposition rates. When deposition rate was 0.05 nm/min, no current through the transistor was observed up to the thickness of 10 nm, where we stopped our measurement. After the deposition of pentacene active layer, the morphology was observed ex situ by an AFM. We compared the morphology of pentacene active layer in the vicinity of metallic contacts between samples treated and not treated with HMDS. The results are shown in Fig. 8.4.



Figure 8.4: Atomic force micrographs of pentacene layer deposited on SiO_2 at a growth rate of 0.05 nm/min. The scan size is $4x4 \ \mu m^2$. The images correspond to pentacene layer thickness of 10 nm. Image 4(a) represents the sample where HMDS treatment was not applied prior to pentacene layer deposition. Black arrows indicate long continuous channel between metallic contact and pentacene layer where no pentacene islands are observed. White arrows indicate rifts in pentacene layer. Image 4(b) represents the sample where HMDS treatment was applied prior to pentacene layer deposition. Black arrows indicate irregularities at metal/pentacene interface.

When surface is not treated with HMDS (Fig. 8.4 (a)) long continuous channel between metallic contact and pentacene layer is observed (indicated with black arrows) where no pentacene islands are observed. The width of the channel ranges up to 500 nm. Similar irregularities in pentacene active layers in the vicinity of metallic contacts are observed also in case when surface was treated with HMDS (Fig. 8.4 (b); indicated with black arrows), but the irregularities are not present all along the metal/pentacene interface as in case presented in Fig. 8.4 (a). In addition, when we compared pentacene layers away from metal/pentacene interface, our results indicate that HMDS also promote adhesion between neighbouring grains in pentacene film. When surface treatment was not performed prior to deposition of pentacene active layer rift in pentacene films were observed (Fig. 8.4 (a); indicated with white arrows). These rifts were not observed when surface was treated with HMDS.

These results indicate that HMDS treatment could be responsible for better adhesion at metal/pentacene interface. As the semiconductor/metal interface plays a crucial role in the performance of OTFT [8, 51], understanding how surface treatment influence the morphology of pentacene active layer near the metallic contact is crucial for understanding of overall performance of OTFT. Our results showed that surface treatment improve the morphology of pentacene layers near the metallic contacts, which could be one of the reasons that higher filed-effect mobility of OTFT is observed when surface treatment is introduced in OTFT fabrication process [11, 38].

8.4 Conclusions

We performed in-situ electrical characterisation of pentacene-based organic thin film transistors, and examined ex situ the morphology of their pentacene channels. By using pentacene growth rates as high as 1.2 nm/min we achieved the field-effect mobility on the order of $0.06 \text{ cm}^2/\text{Vs}$. By using a growth rate 0.05 nm/min two orders lower field-effect mobility was measured. The reduction in mobility with the reduction in growth rate, is coupled in marked change in pentacene layer morphology. Samples fabricated by high growth rate exhibit polycrystalline structure with relatively small grain size. Samples fabricated by a growth rate of 0.05 nm/min exhibit polycrystalline structure with relatively large grain size but with a relatively broad region of uncovered substrate near the metallic contacts of source and drain. This region persisted for pentacene layer thicknesses as high as 10 nm, and is considered to be responsible for lower field-effect mobility and the existence of a plateau in mobility vs. pentacene layer thickness curves. In addition, we investigated the influence of HMDS surface treatment to the morphology of pentacene active layer near the metallic contacts. Our results show that HMDS treatment improves the morphology of pentacene layers at the metal/pentacene interface which could be one of the reasons that higher filedeffect mobility of OTFT is observed when surface treatment is introduced in OTFT fabrication process.

80MORPHOLOGY OF THE METAL-ORGANIC SEMICONDUCTOR CONTACTS: THE ROLE OF

9 Contact resistance in organic thin film transistors

Organic thin film transistors were fabricated by vacuum evaporation of pentacene using different growth conditions in order to tune the pentacene layer morphology. We have performed in situ transport measurements on completed samples, and ex situ morphological characterisation by atomic force microscopy. Electric properties of the microscopic interface environment at the drain/pentacene and source/pentacene interfaces were probed by Kelvin force microscopy. From the observed voltage drops at the metallic contacts we have calculated contact resistances. By decomposing the values into contributions due to injection and due to bulk electric charge transport, we have observed important differences in contact resistance between the samples fabricated by different growth conditions.

9.1 Introduction

Organic thin film transistors (OTFTs) based on polymers and small-molecule organic semiconductors (OSs) attracted much attention in recent years. One of the most thoroughly investigated OS is pentacene [1, 48]. Pentacenebased OTFTs are characterised by a relatively high field-effect mobility ($\sim 1 \text{ cm}^2/\text{Vs}$), which is comparable to the values obtained in amorphous silicon [1, 11, 38, 48]. Satisfactory performance, low manufacturing cost and suitable mechanical properties suggest that pentacene-based OTFTs are likely to become important in large-area electronic applications [1, 48], sensors [100, 101], and organic displays [102, 103, 111].

One of the most commonly used OTFT device geometries is a bottomcontact bottom-gate transistor geometry [48]. In such device a thin organic semiconductor layer is deposited between two coplanar electrical contacts on a suitable insulator substrate, which is in contact with a gate electrode. Most of the present pentacene-based OTFTs are fabricated by vacuum evaporation of a pentacene layer onto a SiO₂-covered highly-doped Si substrate that acts as a gate electrode. Coplanar Au electrodes, separated by a micrometer-long channel act as source and drain contacts [1].

Several studies suggest that the performance of such OTFT is crucially dependent on the morphology of a pentacene layer [9, 11, 24, 38]. A vacuumevaporated pentacene layer on SiO₂ exhibits grains, whose size, shape and crystallographic orientation may vary with the deposition rate [10, 112, 113] and substrate temperature [10, 113]. As for the correlation between the morphology of a pentacene layer and electrical characteristics of an OTFT, a study performed by Shtein *et al.* [11] show that pentacene layers characterised by larger grains exhibit higher field-effect mobility compared to pentacene layers characterised by smaller grains. Similar findings were reported also by Di Carlo *et al.* [9]. Furthermore, Yanagisawa *et al.* [24] showed that in addition to the grain size, also the shape of the grains, and the ratio between the thin film crystalline phase and the bulk crystalline phase play an important role in determining the performance of pentacene-based OTFTs.

The performance of an OTFT may also be affected by the morphological details of the interface between the metal and pentacene near the source and drain contacts. For example, in a study by Kymissis *et al.* [50] and Puntambekar *et al.* [51] a disorder in pentacene layer in the vicinity of electrical source and drain contacts was related to the observed inferior effective field-effect mobility of bottom-contact OTFTs relative to the effective field-effect mobility of top-contact OTFTs. In order to assess the role of microscopic interface environment at the source and drain contacts, Kelvin probe microscopy (KFM) is frequently used, since it allows quantitative mapping of

the electric potential between the source and the drain contacts, during device operation [8, 51, 83, 114, 115]. For example, Puntambekar *et al.* [51] have used KFM to demonstrate that the potential drop at the Au/pentacene is related to the disorder in pentacene layer near the contact.

In this paper we describe a series of experiments that were focused to elucidate the role of a microscopic interface environment on the field-effect mobility in pentacene-based OTFTs. We have performed a systematic study of morphology and electrical properties by atomic force microscopy (AFM) and KFM, respectively, of bottom-contact pentacene OTFTs fabricated under varying growth conditions. Our results indicate a strong correlation between the morphology of the interface at the source and drain contacts and the effective field-effect mobility in OTFTs.

9.2 Experimental

The samples used in our study employed a bottom-gate, bottom-contact geometry of OTFTs [48]. Heavily doped p-type silicon wafers, covered by thermally-grown, 200 nm-thick SiO_2 were used as a substrate. Drain and source metallic contacts were fabricated by thermal evaporation and standard electron-beam lithography and metal lift-off techniques. The contacts comprised 2 nm-thick Ti adhesion layer, covered by 30 nm-thick Au layer. The device channel length was $l = 4 \ \mu m$ and the channel width was $W = 300 \ \mu m$. Upon completion of the lift-off process the SiO_2 surface was cleaned in oxygen plasma to remove residual photoresist from the surface. We have used pentacene that was purchased from Rieldel-de Han and was not additionally purified. Pentacene was evaporated in a high-vacuum chamber, with the base pressure of $1 \cdot 10^{-5}$ Pa. We have examined samples fabricated under three different combinations of deposition rate (r), and substrate temperature T_{sub} . In what follows we will address the samples fabricated under a selected pair of growth parameters as Type I, Type II or Type III. Samples of Type I were fabricated using r = 0.7 nm/min and T_{sub} = 80°C, samples of Type II were fabricated using r = 0.75 nm/min and $T_{sub} = 50^{\circ}$ C, and samples of Type III were fabricated using r = 1.6 nm/min and $T_{sub} = 80^{\circ}$ C. The thickness of the pentacene layer was 45 nm for all samples. The thickness was determined in situ using quartz thickness monitor, and ex situ by AFM.

Upon completion of the deposition of the pentacene layer we have performed electrical characterisation of OTFTs in situ. The source, the drain, and the gate contacts were connected to the power supply (Keithley 6487) and to the ammeter (Keithley SourceMeter 2400) via an electrical vacuum feed-through. Subsequently, we have examined the morphology and electrical properties of the samples ex situ by AFM and KFM using Veeco CP-II scanning probe microscope. During the preparation of electrical contacts (adjusting electrical wires with electrical contacts on the samples), we kept the samples in a N2 atmosphere. During data acquisition the samples were kept in air but under a controlled humidity (50%) and temperature (23°C - 25°C). We have used Olympus platinum-coated silicon probes (Rf = 70 kHz; spring constant = 2 N/m). The KFM and AFM signal were recorded simultaneously during the scan.

9.3 Results and discussion

Fig. 9.1 shows OTFT transfer characteristics measured in situ after deposition of the pentacene layers for three representative samples. Different curves correspond to different growth conditions, curve (a) corresponds to samples of Type I, curve (b) corresponds to samples of Type II, and curve (c) corresponds to samples of Type III. In the inset of figure 1 we show typical current-voltage (I-V) characteristics obtained for the OTFT of Type I, presented in the main figure.

The effective field-effect mobility values were calculated from the transfer characteristics and I-V curves in the saturation regime, following the model frequently used to predict the operation of inorganic transistors [25]. The values of effective field-effect mobility for the sample of Type I was 0.05 cm²/Vs, for the sample of Type II was 0.09 cm²/Vs, and for the sample of Type III was 0.16 cm²/Vs.

From these results we may conclude that the growth parameters are important for the performance of OTFTs devices. The field-effect mobility of the sample of Type III (r = 1.6 nm/min) is more than three times higher than the field-effect mobility of the sample of Type I (r = 0.7 nm/min), and almost twice the field-effect mobility of the sample of Type II (r = 0.75 nm/min). Moreover, the increase in T_{sub} results in a decrease in the field-effect mobility at fixed r (Type I vs. Type II). Yanagisawa *et al.* [24] observed a field-effect mobility that was a decreasing function of substrate temperature above 50°C. In addition, Ref. [24] also shows that in order to increase a field-effect mobility of the samples fabricated at higher substrate temperatures, a higher evaporation rate is preferred.

In what follows we present morphological and KFM results obtained on these samples. Fig. 9.2 shows the morphology of pentacene layer evaporated at different growth parameters in the transistor channel. The thickness of pentacene layer presented in figure 2 is 45 nm in all cases.

Fig. 9.2 (a) represents sample Type I, for which pentacene was deposited



Figure 9.1: In situ transfer characteristics measurements obtained at drain voltage $V_d = -1$ V for samples where pentacene active layer was deposited at different evaporation conditions. The evaporation conditions were as follows: (a) sample Type I: r = 0.7 nm/min and $T_{sub} = 80^{\circ}$ C, (b) sample Type II: r = 0.75 nm/min and $T_{sub} = 50^{\circ}$ C, and (c) sample Type III: r = 1.6 nm/min and $r = 80^{\circ}$ C. The inset exemplifies current voltage characteristics (I-V) measured on sample Type I.

at high temperature and low evaporation rate. Pentacene layer morphology of Type I is characterised by defects that are present inside the channel (black arrows) and near the metallic contact (white arrows). At the Au/pentacene interface we observe smaller grain size than inside the channel. In addition, we observed regions, where no extended pentacene islands were present. Furthermore, inside the channel we observe large grains (perimeter of up to 2μ m) relative to the grains near the interface. We also observe relatively wide trenches, where no extended pentacene islands are present. The depth of observed trenches measured with AFM ranges from 40nm to 45nm, which is a nominal thickness of the pentacene layer.

Fig. 9.2 (b) shows the morphology of the pentacene layer for the sample Type II (growth rate of 0.75 nm/min, and substrate temperature of 50°C). We see that the layer is continuous, albeit with varying grain size with perimeter ranging from 0.400 μ m to 1.5 μ m. Moreover, the boundaries between neighboring grains are not separated with broad trenches as is the case of the Type I samples.

Pentacene layer morphology observed in Fig. 9.2 (c) represents sample Type III (growth rate of 1.6 nm/min, and substrate temperature of 80°C). Also here we observe a continuous layer with no trenches as in the case of

86 CONTACT RESISTANCE IN ORGANIC THIN FILM TRANSISTORS



Figure 9.2: AFM images of pentacene layer inside the transistor channel. The scan size of each image is 6 μ m. The thickness of pentacene layer is 45 nm in all cases. Brighter areas indicate the location of the metallic layers. (a) AFM image of a pentacene layer inside the transistor for sample Type I (r = 0.7 nm/min; T_{sub} = 80°C), (b) sample Type II (r = 0.75 nm/min; T_{sub} = 50°C), and (c) sample Type III (r = 1.6 nm/min; T_{sub} = 80°C). White arrows in image (a) point to defects in the pentacene layer at the Au/pentacene interface. Black arrow in image (a) points to defects in the pentacene layer away from the metallic contacts.

sample Type I. Fig. 9.2 (c) shows smaller grains at the Au/pentacene interface, but not to the extent observed in Fig. 9.2 (a). An average grain size observed in the image is 2 μ m \pm 0.5 μ m (Fig. 9.2 (c)).

When comparing the results of electrical characterisation (Fig. 9.1) with morphological images of the samples of all three types (Fig. 9.2), we see the
correlation between the morphology and OTFT device performance. Type I sample shows the lowest effective field-effect mobility. The morphology of pentacene layers for sample Type I is characterised by defects in the pentacene layer both inside the channel, and at the Au/pentacene interface. We have seen that the trenches may reach the substrate (Fig. 9.2 (a)). However, based on the resent reports that electric charge transport in OTFTs occurs along first two molecular layers of pentacene [52, 98, 108] we can conclude that also defect that do not reach the SiO₂ may have a detrimental effect on the on electric charge transport across the channel.

Pentacene layers of samples of Type II and Type III (Fig. 9.2 (b) and (c), respectively) are free of defects in the form of trenches. The difference in morphology of pentacene layers for both samples is observed inside the transistor channel far from the contacts. The morphology of Type II sample is characterised by substantially smaller grains. This could be the reason for lower field-effect mobility measured for the Type II samples [9, 11].

The observed correlation between the morphology and electrical parameters of the OTFTs was further investigated with the KFM measurements. Fig. 9.3 shows surface potential curves, corresponding to different drain (V_d) and gate voltages (V_g) applied to the electric contacts during the scan on sample Type I. Curves correspond to $V_d = V_g = -15$ V, $V_d = V_g = -10$ V and $V_d = V_g = -5$ V, top to bottom, respectively. During a KFM scan, morphological features of a pentacene layer may affect the recorded values of the surface potential. This is especially important at the metal/pentacene interface where structural disorder is likely to be present. (See for example Fig. 9.3 (a)). In order to avoid such artifacts we have performed KFM scans for different gate voltages along the same scan line. Furthermore the location of the scan line was selected so that the interface voltage drop was the smallest.

From the surface potential curves we have obtained values of voltage drops at the source/pentacene interface (ΔV_s) , drain/pentacene interface (ΔV_d) and along the channel (ΔV_{ch}) . We note, that marked difference in the voltage drop is observed at the source/pentacene interface compared to the drain/pentacene interface. Similar difference in the voltage drop on Au/pentacene interfaces was observed also by Puntambekar *et al.* [51] on bottom-contact pentacene-based OTFTs, and by Bürgi *et al.* [8] on vapourdeposited polymer OTFTs. The asymmetry in the voltage drop between source and drain was related by Bürgi *et al.* [8] to different contribution of injecting resistance (\mathbf{R}_i) to the overall resistance of the device. The authors separated the conduction path between the source and drain into series of four resistive elements: $\mathbf{R}_{s-d} = \mathbf{R}_i + \mathbf{R}_b + \mathbf{R}_{ch} + \mathbf{R}_b$. The origin of \mathbf{R}_b was ascribed to the defects in the semiconductor layer in the vicinity of source and drain electrical contacts. R_{ch} is the gate-modulated channel resistance. Since the type and density of the defects in the semiconductor layer near both metallic contacts is expected to be equal, the contribution of R_b is the same at both contacts. On the other hand, R_i is present only at the source contact resistance, since the origin of R_i is a charge carrier injection at the reverse-biased source contact. Therefore, the value of R_i is closely related to the hole injection barrier at the Au/pentacene interface. Since the energy barrier is relatively high (0.47 eV) [19] the contribution of R_i is expected to be significant [8]. On the other hand, the resistance arising from the extraction of charge carriers at the forward biased drain is expected to be negligible. The resistance at the drain contact is therefore mainly due to bulk resistance (R_b) resulting in much smaller drain contact resistance compared to the source contact resistance.

In order to investigate these issues, we have calculated R_s , R_d , and R_{ch} for all three sample-types at different values of $V_g - V_t$, with V_t representing a threshold voltage. The values for R_s were calculated as $R \cdot W$, where $R = \Delta Vs/I_{sd}$, I_{sd} is the source-drain current through the transistor, ΔV_s is



Figure 9.3: Surface potential profiles obtained for the sample Type I (r = 0.7 nm/min; $T_{sub} = 80^{\circ}\text{C}$). Different surface potential curves correspond to different drain (V_d) and gate voltages (V_g) applied to the electric contacts during the scan. Curves correspond to $V_d = V_g = -15 \text{ V}$, $V_d = V_g = -10 \text{ V}$ and $V_d = V_g = -5 \text{ V}$, from the top to bottom, respectively. All potential profiles were taken within 2 μ m along the transistor channel.



Figure 9.4: Drain (\mathbf{R}_d) , source (\mathbf{R}_s) , and channel (\mathbf{R}_{ch}) resistance as a function of \mathbf{V}_g - \mathbf{V}_t (a, b and c, respectively) for Type I (squares), Type II (circles) and Type III (triangles) samples. The insets in (a), (b) and (c) show the voltage drops measured at drain/pentacene interface, source/pentacene interface, and in the transistor channel.

the voltage drop at the source/pentacene interface, and W is the channel width (W = 300 μ m). The values for R_d were calculated as $R \cdot W$, where R= $\Delta V_d/I_{sd}$, and ΔV_d is the voltage drop at the drain/pentacene interface. The values for R_{ch} were calculated as $R \cdot (W/l)$, where $R = \Delta V_{ch}/I_{sd}$, ΔV_{ch} is the voltage drop across the channel, and (W/l) is the ratio between the channel width and the channel length (l = 4 μ m). The results are presented in Fig. 9.4, where we show the resistance R_d , R_s , and R_{ch} , as a function of $V_g - V_t$ (Fig. 9.4 (a), (b) and (c), respectively). The results of Type I sample are presented by squares, the results of Type II are presented by circles and the results Type III are presented by triangles.

We see that the highest resistance at the drain/pentacene interface is present at the sample that exhibited the highest degree of structural disorder (Fig. 9.2 (a), and Fig. 9.4 (a)-squares). On the other hand the samples with relatively similar interface morphology (Fig. 9.2 (b) and (c)) exhibit almost no variation in R_d . Focusing on Fig. 9.4 (b) we see, that the highest resistance at source/pentacene interface is present at the Type I samples, but substantial difference in Rs between Type II and Type III samples is observed. We interpret these result using the approach suggested by Bürgi et al. [8]. Consistently higher R_d in the case of sample Type I is a consequence of increased interface disorder and thereby increased contribution of R_b . On the other hand similar resistance of samples with similar morphology indicates also similar contribution of R_b in these samples. At the source/pentacene interface, where the contribution of R_i becomes important, the R_b in sample Type I is still apparent. However, differences in Rs between Type II and Type III become visible, and may be due to structural, chemical and/or electronic details at the interface that are difficult to probe at the pentacene thickness employed in our experiments.

The role of increased disorder in determining channel resistance becomes clear in Fig. 9.4 (c), where the contribution of R_i should be negligible, and the only contribution to the resistance is due to R_b . We see that the channel resistance of Type I samples is the highest, which is consistent with observed high degree of structural disorder (Fig. 9.2 (a)). Less obvious morphology/mobility correlation is present in the case of the samples of Type II and Type III, which both exhibit similar morphology, but differ considerably in effective field-effect mobility. Only through the use of KFM we can probe detailed nature of channel and contact resistance and draw conclusions regarding superior performance of Type III samples. While both sample types exhibit similar resistance inside the channel at higher values of $V_g - V_t$, their source contact resistance differs almost for factor of four for all values of $V_g - V_t$.

9.4 Conclusion

In conclusion, we performed in situ characterization of the organic thin film transistors where pentacene layer was deposited at different deposition conditions. Morphology of the samples was investigated by the AFM. Results of AFM measurements showed that deposition conditions influence the morphology of pentacene layer in the vicinity of Au/pentacene interface as well as inside transistor channel. Simultaneous use of Kelvin force microscopy and AFM allowed us to probe the electric properties at the source and drain interface with pentacene. By using the electric-potential vs. position curves we were able to extract important differences in interface voltage drops between the samples fabricated by different growth conditions. We can explain the observed differences in terms of different contributions to the overall resistance that stem from injection and bulk electric charge transport.

9.5 Acknowledgements

We thank G. Horowitz for fruitful suggestions. Cheerful assistance of P. Rebernik Ribič is also acknowledged.

92 CONTACT RESISTANCE IN ORGANIC THIN FILM TRANSISTORS

10 Lifetime of organic thin film transistors: oxygen doping vs. water diffusion

Time-depended electric charge transport measurements of pentacene organic thin film transistors (OTFTs) coupled to Kelvin force probe microscopy, demonstrate that exposure of OTFTs to ambient air for extended periods of time, results in two competitive mechanisms that are responsible for observed variation in drain-current. Initially, relatively fast oxygen doping through electronegativity-related creation of holes increase the carrier concentration, and hole barrier lowering at the source/pentacene promote the charge injection from metallic contact into semiconductor layer and therefore increases the drain current. Slower, and persistent mechanism of water diffusion in the pentacene layer induces dipole-charge carrier interactions through the creation of energetic disorder. These results in long-term reduction of sourcedrain current.

10.1 Introduction

In recent years organic semiconductors (OSs) attracted much attention in the field of organic electronics. The main attributes of OSs are low temperature processing, mechanical flexibility and applicability for large area devices fabrication [7, 48, 116]. However, when exposed to ambient air the electrical and in some cases morphological stability of OS based devices is affected [12, 117–119]. While in some cases degradation of device performance in ambient air is problematic, since the life-spent of devices is affected, sensitivity to air gases and light could be exploited for fabrication of OSs based sensors. In either case, understanding of air gases influence, to the performance of OSs based devices, is the key issue.

One of the most promising materials for organic electronic is pentacene due to the high charge carrier mobility measured in pentacene based organic thin film transistors (OTFTs) [38, 39] and possibility to control the growth of thin films by the means of the substrate temperature and deposition rate [10, 24, 113]. A vacuum-evaporated pentacene layer on SiO₂ exhibits polycrystalline structure, where size of grains vary between hundreds of nanometers up to a few microns, depending on the deposition conditions [10, 24].

Critical factor influencing the charge transport in OTFTs is π -orbital overlap between pentacene molecules [120, 121]. In these regards, grain boundaries should prove an obstacle for electric charge to transfer from one grain to another. Therefore, increasing grain boundary density should act as deteriorative factor of charge transport in OTFTs [9].

Resistance at the metal/OS interfaces is another factor governing the charge transport in OTFTs. This so-called contact resistance can limit or even control the charge transport in OTFTs [8, 51, 114, 115]. According to Bürgi et al. [8] there are two contributions influencing the contact resistance. First is ascribed to the defects in the semiconductor layer in the vicinity of source and drain electrical contacts and the second is originated from the carrier injection at the reverse-biased source contact, and therefore, closely related to the hole injection barrier at the OS/metal interface [8]. The influence of contact resistance to the overall performance of the OTFTs was in recent years studied by several groups employing a Kelvin force probe microscopy (KFM) [8, 51, 114, 115]. The technique was used to determine the contact resistance between different OSs and electrical contacts fabricated from different materials [8, 114, 115]. Disorder in pentacene layer in the vicinity of electrical source and drain contacts was investigated by comparing the bottom-contact and top-contact OTFTs. Superior performance of the latter was related to the disorder of OSs layers in the vicinity of metallic contacts, observed only in case of bottom-contact OTFTs [51].

When pentacene based OTFTs are exposed to air, two competitive mechanisms involving the presence of oxygen and humidity are influencing the charge transport in OTFTs. Absorbed oxygen enhances the conductance in pentacene active layer by introducing holes near the valence band [13]. In addition, Vollmer et al. [122] showed that the pentacene/Au hole injection barrier is affected and is lowered for 0.25 eV upon exposition to oxygen, which should substantially decrease the contact resistance at the source/metal interface, and therefore improve the charge carrier injection from the source contact to the OS layer [8]. In contrast, humidity is responsible for formation of trapping sites which are responsible for reduction of free charge carriers and thus for degradation of electrical performance in OTFTs [13, 117, 123]. In addition, theoretical approach was taken to explain the influence of additional H atom in the pentacene molecule system to electric charge transport. Results show that perturbation of carbon atom, converting a C-H unit to a $C-H_2$ unit results in p_z orbital removal and therefore rise to a state in the gap [121].

In this work we investigated the influence of the ambient air exposure to the performance of pentacene-based OTFTs by employing the KFM technique. KFM measurements allowed us to follow the evolution of resistance in time at the source/pentacene, the drain/pentacene and inside the channel, separately. Consequently, we were able to determine which part of transistor was more sensitive and thus responsible for the degradation in charge transport after the prolonged exposure to ambient air.

10.2 Experimental

We have used a bottom-gate, bottom-contact geometry of OTFTs in our experiment. The substrates comprised heavily doped p-type silicon wafers, covered by thermally-grown, 200 nm-thick SiO₂. Metallic contacts were fabricated by combined electron and optical lithography. The contacts comprised 2 nm-thick Ti adhesion layer, covered by 30 nm-thick Au layer. The device channel length was $l = 4 \ \mu m$ and the channel width $W = 300 \ \mu m$. Upon completion of the lift-off process the SiO₂ surface was cleaned in oxygen plasma to remove residual photoresist from the surface. We have used pentacene purchased from Rieldel-de Han, and it was not additionally purified. Pentacene was evaporated in high vacuum, at the residual pressure of $1 \cdot 10^{-5}$ Pa. The deposition rate was 2 nm/min and the substrate temperature T_{sub} = 60°C. The thickness of the pentacene layer was 50 nm. The thickness was measured in situ using quartz thickness monitor, and ex situ by atomic force microscopy (AFM).

After the deposition of pentacene layer, we examined the morphology and electrical properties of the samples ex situ by AFM and KFM using Veeco CP-II scanning probe microscope. During the preparation of samples for electrical and KFM measurements, we kept the samples in a N₂ atmosphere. The source and the drain contacts were connected to an amperemeter (Keithley SourceMeter 2400), and the gate contact was connected to a power supply (Keithley 6487). During the KFM measurements we kept the samples under ambient air with humidity varying between 61% and 66%. We have used Olympus platinum-coated silicon probes (Rf = 70 kHz; spring constant = 2 N/m). The KFM and AFM signal were recorded simultaneously during the scan.

10.3 Results and discussion

Fig. 10.1 shows the source-drain current (I_{sd}) evolution in time (filled squares) for OTFTs exposed to ambient air. The time scale indicated in the figure corresponds to time that elapsed from the moment the N₂ supply was turned off. The values of the I_{sd} shown in the figure correspond to average value of 15 measurements obtained during the KFM measurements, with the gate voltage $V_g = -10$ V, and the drain voltage $V_{sd} = -10$ V. In Fig. 10.1 we also show the time evolution of the threshold voltage (V_{th}) (filled circles). The threshold voltage was calculated from a transfer curve for a drain voltage $V_{sd} = -1$ V. The transfer electrical characterisations were always performed immediately after the KFM measurements.

During a period of six hours from the moment the N₂ supply was turned off, we observed a rapid increase in I_{sd} . After the initial increase, a more gradual decrease of I_{sd} was observed. The behaviour of I_{sd} was first coupled to variation of threshold voltage V_{th} (Fig. 10.1, filled circles). During the initial period we observed strong variations of V_{th} , while at the onset of decrease in I_{sd} , V_{th} started a monotonic increase. In order to gain insight into the behavior of I_{sd} , we adopt gradual channel approximation (GCA) [124] in which $I_{sd} \sim (V_g - V_{th})^2$ in the saturation regime of the transistor operation. In GCA, V_{th} depends on doping level of the substrate, interface barrier and the capacitance of the insulator. Therefore, the observed coupling of the changes in I_{sd} to the changes in V_{th} are to be sought in the effects of doping of the pentacene layer as a consequence of exposure of OTFTs to ambient air.

The tendency of threshold voltage shift towards the positive values after exposure to ambient air was recently reported by Kumaki *et al.* [79]. They associate observed shift in V_{th} towards positive values to the accumulation



Figure 10.1: The time evolution of source-drain current (filled squares) and the time evolution of threshold voltage (filled circles) for OTFTs exposed to air.

of the holes inside the channel, which was observed even for the $V_g \ge 0$ V. The presence of accumulated holes was attributed to the influence of trap sites formed at the SiO₂/pentacene interface and at the grain boundaries. The traps were generated by the chemical reactions between the oxygen and water molecules and the SiO₂ surface.

Our data in Fig. 10.1 (filled circles) indeed showed a gradual increase in V_{th} with time. While the increase in V_{th} was initially coupled with a sharp increase in I_{sd} , the latter began a descent after about less than 10h, despite a monotonic increase in V_{th} . Further insight into such behaviour was obtained by KFM measurements that are exemplified in Fig. 10.2, which shows an AFM image of the pentacene layer (a) and KFM surface potential profiles as a function of time (b). The profiles were obtained in the region indicated in Fig. 10.2 (a) by a rectangle. Brighter areas in the AFM image indicate the location of the metallic contacts. The pentacene active layer was characterised by grains with size in the range from 0.5 μ m to 2 μ m. We see that the layer morphology changed near the metallic contacts, where we observed a considerable reduction in the grain size.

We have performed KFM scans 5 min, 1.5h, 4.1h, 6 h, 29 h and 47 h, after the N₂ supply was turned off. From the profiles presented in Fig. 10.2 (b) we can determine the voltage drops at the source/pentacene contacts (ΔV_s), drain/pentacene contacts (ΔV_d) and inside the transistor channel (ΔV_{ch}).



Figure 10.2: AFM image of the pentacene layer (a) and surface potential profiles as a function of time (b). The size of scanned area is 7 μ m. The thickness of pentacene layer used in our experiment is 50 nm. Brighter areas in the AFM image indicate the location of the metallic contacts. Rectangle in the AFM image indicates the place, where the KFM imaging was performed. The gate voltage during the scan was $V_g = -10$ V and the drain voltage was $V_{sd} = -10$ V. The surface potential profiles were taken 5 min, 1.5h, 4.1h, 6 h, 29 h and 47 h, after the N₂ supply was turned off, from the bottom to the top curve, respectively.

RESULTS AND DISCUSSION

In Fig. 10.3 we summarise the calculated values of these quantities as a function of time. Each value was an average of 6-8 measurements taken during the measurement. We can observe a share decrease of ΔV_s , and a sharp increase of ΔV_{ch} within the first 10h, after the moment the N₂ supply was turned off. On the other hand ΔV_d increases monotonically in time, throughout the duration of the experiment. The general observation of time evolution presented in Fig. 10.3 is that the voltage drop at source contact was dominant but becomes smaller as the voltage drop inside the channel increases.

In order to evaluate the time evolution of contact resistance, we combined the measurements of I_{sd} (Fig. 10.1) with the voltage drops shown in Fig. 10.3. We calculated source resistance (R_s) , drain resistance (R_d) and channel resistance (R_{ch}) . The values for R_s were calculated as $R_s = \Delta V_s \cdot W/I_{sd}$, with W as the channel width (W = 300 μ m). The values for R_d were calculated as $R_d = \Delta V_d \cdot W/I_{sd}$. The values for R_{ch} were calculated as $R_{ch} = \Delta V_{ch} \cdot (W/1)/I_{sd}$, with (W/1) as the ratio between the channel width and the channel length (W/1 = 75). The results are presented in Fig. 10.4, where we show the resistance R_d , R_{ch} , and R_s , as a function of time (Fig. 10.4 (a), (b) and (c), respectively). R_s exhibits more than a factor of three decrease during the first 6 hours, after the moment the N₂ supply was turned off. After that, R_s



Figure 10.3: Time evolution of voltage drops on source/pentace contact (indicated with squares), inside transistor channel (indicated with circles) and on drain/pentacene contact (indicated with triangles).

is almost constant in time. Both, R_{ch} and R_d exhibit an initial drop followed by the increase. The relative increase of R_d (2.5-times) is slightly higher than the increase of R_{ch} (2-times). From the fact that R_{ch} and R_d exhibit similar time evolution, we may conclude that exposure to ambient air has similar effect to the electronic transport properties of a pentacene layer inside the channel, and on the pentacene/drain interface.

In order to explain the influence of ambient air to the R_s , R_{ch} and R_d and thus the observed time evolution of current, we will use the model proposed by Bürgi *et al.* [8]. The authors suggested that the conduction path between the source and drain should be divided into series of four resistive elements: $R_{s-d} = R_i + R_b + R_{ch} + R_b$. The origin of R_b was ascribed to the defects in the semiconductor layer in the vicinity of source and drain electrical contacts, R_{ch} is the gate-modulated channel resistance and the origin of R_i is a charge carrier injection at the reverse-biased source contact and therefore, the value of R_i is closely related to the hole injection barrier at the Au/pentacene interface. Therefore, $R_d = R_b$, which means that the time evolution of R_d observed in our experiment must be explained in terms of R_b . Fig. 10.2 (a) shows an increased density of the grain boundaries in the vicinity of electrical contacts. Such alteration of morphology could be related to the change in electronic properties relative to the electronic properties within the channel, away from the contacts. R_b may therefore arise from an increased density of the grain boundaries near the pentacene/Au interface. The fact was proven by Puntambekar et al. [51] by comparing the contact resistance of bottom-contact and top-contact pentacene based OTFTs. Results of the experiment showed a marked difference in a contact resistance between both geometries and the difference was related to the pentacene morphology at the pentacene/Au interface. In the case of top-contact transistors larger grain size and consequently smaller contact resistance was reported. As for the time evolution of R_d we attribute its behaviour to two combined processes: oxygen and water absorption. The two types of molecules were found to have opposing effects on transport of electric charge through pentacene layers. Jurchescu et al. [13] have performed a systematic analysis of the effect of air exposure on the electronic properties of pentacene single crystals. Exposure of the samples to dry air resulted in an increase of measured current between the metallic contacts, whereas exposure to humid air resulted in a decrease of current between the metallic contacts. Similar effect of water exposure was found also by also Zhu et al. [125] who used pentacene-based OTFTs as humidity sensors. Oxygen doping of pentacene has the effect of stripping-off the electrons from the molecules. Consequently, additional holes are created within the layer, increasing thereby the density of free charge carriers and increasing the effective conductivity of the layer. On the other hand, water



Figure 10.4: Time evolution of drain resistance (R_d) , channel resistance (R_{ch}) and source resistance (R_s) for time intervals: immediately after the samples were exposed to ambient air, after 1.5 h, 4.1 h, 6 h, 29 h and after 47 h exposition (Figures 4(a), 4(b), 4(c), respectively).

molecules may enter the pentacene layer via grain boundaries and reach the first two molecular layers of pentacene, responsible for the charge transport in OTFTs [52, 98]. Water molecules affect the transport of the charge carriers through charge-dipole interactions that cause an important dependence of the charge mobility on the applied field and introduce a disorder in the energy distribution of the states responsible for the charge transport [126]. The overall effect of water exposure is therefore a drop in charge carrier effective mobility.

Based on these findings we interpret the initial reduction in R_d observed in our experiment (Fig. 10.4 (a)) in terms of absorbed oxygen which enhances the conductance in pentacene active layer [13]. As the time progresses an increasing concentration of water molecules penetrates the pentacene layer. This process is slower than the oxygen doping due to hydrophobic nature of pentacene molecules, but eventually dominates. This is evidenced by a monotonic increase in R_d after 4.1 h exposition to air. Similar time evolution is also observed in the case of R_{ch} (Fig. 10.4 (a) and (b)). Therefore, we assume that the same rationale can be employed for explaining the behaviour of R_{ch} .

In contrast to R_d and R_{ch} different time evolution is observed for R_s (Fig. 10.4 (c)). In terms of model proposed by Bürgi *et al.* [8], R_s should be described as $R_s = R_b + R_i$. Since the morphology of semiconductor layer near source and drain metallic contacts is equal (confirmed by AFM image in Fig. 10.2 (a)), the contribution of R_b is the same at both contacts. Fig. 10.4 shows that the drop of R_s within the first 6 hours, after moment the N_2 supply was turned off, is approximately 10-times higher than the value of R_d . This means, that the term R_b may be neglected in interpreting the origin of R_s , and only R_i may be taken into account. R_i depends on the detailed nature of the charge carrier injection process at the reverse-biased source contact. The energy barrier between the Fermi level in Au contact and pentacene highest occupied molecular orbital measured in vacuum amounts to 0.47 eV [19]. Vollmer *et al.* [122] showed that due to the modification of Au surface properties the pentacene/Au energy barrier may be lowered by 0.25 eV after the exposition of samples to oxygen. The lowering of the injection barrier should decrease the value of R_i and thus decrease the value of R_s as measured in our experiment (Fig. 10.4 (c)).

After the initial drop of R_s within the first 6 hours a slight increase in R_s is observed. The relative change of R_s , due to the increase is small, nevertheless, the measured increase between the fourth point (6 hours after N_2 was turned off) and sixth point (47 hours after N_2 was turned off) is $2.4 \cdot 10^4 \ \Omega$ cm. This change of R_s is very close to the change of R_d between the third point, when minimum value of R_d is reached (4.1 hours after N_2

was turned off) and sixth point (47 hours after N₂ was turned off), which is $3 \cdot 10^4 \ \Omega$ cm. This may be an indication, that source/pentacene interface is also affected by the presence of humidity, but the major contribution to the time evolution of R_s is initial lowering of the hole injection barrier which is result of surface modification of Au due to the presence of oxygen.

10.4 Conclusion

We investigated the influence of the pentacene-based OTFTs exposure to ambient air. The current flow through the transistor depends upon the properties of active layer and source/OS/drain interfaces. Kelvin force microscopy was used to investigate the influence of ambient air to each of above components. The major contribution to the current transport through the transistor is attributed to the hole barrier lowering at the source/pentacene interface due to oxygen- modified Au surface, resulting in smaller value of source contact resistance and thus increasing current observed in our measurements. After longer exposition source resistance is also affected by the humidity, but the contribution is relatively small inside the time-frame of our experiment. Different behaviour is observed for channel and drain resistance. Although the presence of oxygen decreases the resistance, the effect is present only for a short period of time, after which the opposite trend is observed. The increase in resistance is attributed to the formation of traps due to presence of humidity. 104LIFETIME OF ORGANIC THIN FILM TRANSISTORS: OXYGEN DOPING VS. WATER DIFF

11 Conclusions

In the first part, our work was focused on the fabrication and optimisation of the source-drain metallic contacts by different methods of microlithography. The electrical source-drain contacts in our experiment comprised 3 nm-thick or 2 nm-thick Ti adhesion layer, and 30 nm to 50 nm-thick Au layer, evaporated on the top of Ti layer. OTFTs channel lengths ranged between 4 μm and 5 μm and the channel widths ranged between 0.3 mm and 2.3 mm. Initially, we prepared the electrical contacts by using the single layer optical lithography. The samples were prepared by deposition of photoresist on top of the substrate, exposure of a photoresist with UV light through the chromium mask, development of a photoresist, deposition of a metal on top of the substrate, and removal of the residual photoresist by immersing the samples into hot acetone or remover (LIFT-OFF process). Results showed that the method was not suitable for sample preparation in our experiment, since the excess Au material very often remained at the edges of the sourcedrain contacts. The problem was overcame by using double layer optical lithography or electron-beam lithography.

The influence of Ti adhesion layer on the electric charge transport in OTFTs was investigated by following the evolution of source-drain current (I_{sd}) during the evaporation of pentacene layer. The electric source-drain contacts in the experiment were prepared by employing 3 nm-thick, 2 nm-thick, and control samples without Ti adhesion layer. We associated the delayed onset of I_{sd} , for the OTFTs fabricated with the thick Ti adhesion layers, with the high hole injection barrier at Ti/pentacene interface. The onset of current in these OTFTs was observed only after the nominal thickness of pentacene layer was close to the thickness of Ti adhesion layer, and so enabling the charge injection from the Au layer into pentacene. The delayed onset of current was not observed, if the samples were prepared using only 2-nm thick Ti adhesion layer. Based on these results, we estimated the critical thickness of Ti adhesion layer to ~ 2 nm. In addition, based on the morphological observation of pentacene layers and the evolution of source-drain current, we concluded that the majority of mobile charge, and therefore,

the thickness of transport layer is limited inside the first-two monolayers of pentacene.

Further work involved the systematic investigated of the role of SiO_2 surface treatment on pentacene morphology at the Au/pentacene interfaces. The substrates included as-grown SiO_2 and SiO_2 surface treated by HMDS. The resulting OTFTs were investigated in situ, during growth of pentacene layer by measuring the I_{sd} , and ex situ by AFM. Our results showed that the effective field-effect mobility of OTFTs decreased with decreasing deposition rate. By using deposition rates as high as 1.2 nm/min we achieved the field-effect mobility on the order of $0.06 \text{ cm}^2/\text{Vs}$. By using a growth rate 0.05 nm/min two orders lower field-effect mobility was measured. Morphological investigation of pentacene layer deposited at low deposition (~ 0.05 nm/min) rates showed an existence of discontinuous pentacene coverage at the Au/pentacene interface. We associate the decrease in mobility to this morphological feature. We have found that the HMDS treatment results in a reduced areal density of extended structural defects. However, at the lowest growth rates even HMDS treatment can not promote wetting of the Au contacts with pentacene in order to close the gap between pentacene and the Au contact.

Further work was carried out to investigate the influence of the substrate temperature on the field-effect mobility in pentacene-based OTFTs. We have examined samples fabricated under three different combinations of deposition rate (r), and substrate temperature (T_{sub}) . In what follows we will address the samples fabricated under a selected pair of growth parameters as Type I, Type II or Type III. Samples of Type I were fabricated using r = 0.7nm/min and $T_{sub} = 80^{\circ}$ C, samples of Type II were fabricated using r = 0.75nm/min and $T_{sub} = 50^{\circ}$ C, and samples of Type III were fabricated using r = 1.6 nm/min and $T_{sub} = 80^{\circ}$ C. In the first part of the experiment, we have performed in situ transport measurements on completed samples, and ex situ morphological characterisation by AFM. In situ electrical measurements showed the lowest field-effect mobility for the Type I samples, which was attributed to the pentacene layer morphology characterised by defects present inside the transistor channel and near the metallic contact. Less obvious morphology/mobility correlation is present in the case of the samples of Type II and Type III, which both exhibit similar morphology, but differ considerably in field-effect mobility, therefore, additional characterisation followed by KFM. Only through the use of KFM we were able to detailedly probe the nature of channel and contact resistance and draw conclusions regarding superior performance of Type III samples. Results showed that while both sample types exhibit similar resistance inside the channel, their source contact resistance differs almost for factor of four, resulting in higher field-effect mobility of Type III samples.

In the final part of our work we investigated the influence of air exposure on the electrical performance of pentacene-based OTFTs. Time-depended electric charge transport measurements of pentacene-based OTFTs coupled to KFM, demonstrated that exposure of OTFTs to ambient air for extended periods of time, results in two competitive mechanisms that are responsible for observed variation in I_{sd} . Initially, relatively fast oxygen doping through electronegativity-related creation of holes increase the carrier concentration, and hole barrier lowering at the source/pentacene promote the charge injection from metallic contact into semiconductor layer and therefore increases the drain current. Slower, and persistent mechanism of water diffusion in the pentacene layer induces dipole-charge carrier interactions through the creation of energetic disorder. These results in long-term reduction of I_{sd} . KFM measurements allowed us to follow the evolution of resistance in time at the source/pentacene, the drain/pentacene and inside the channel, separately. Consequently, we were able to determine which part of OTFTs was more sensitive and thus responsible for the alteration in charge transport properties after the prolonged exposure to ambient air.

CONCLUSIONS

Bibliography

- C. D. Dimitrakopoulos and P. R. L. Malenfant, Adv. Mater. 14, 99 (2002).
- [2] S. R. Forrest and M. E. Thompson, Chem. Rev. **107**, 953 (2007).
- [3] M. M. Ling and Z. Bao, Chem. Mater. **16**, 4824 (2004).
- [4] N. Karl, Syn. Met. **133-134**, 649 (2003).
- [5] E. Pavlica and G. Bratina, Phys. Stat. Sol.(b) **243**, 473 (2006).
- [6] R. Hudej and G. Bratina, J. Appl. Phys. **93**, 6090 (2003).
- [7] A. R. Brown, C. P. Jarrett, D. M. de Leeuw, and M. Matters, Syn. Met. 88, 37 (1997).
- [8] L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, J. Appl. Phys. 94, 6129 (2003).
- [9] A. D. Carlo, F. Piacenza, A. Bolognesi, B. Stadlober, and H. Maresch, Appl. Phys. Lett. 86, 263501 (2005).
- [10] S. Pratontep, M. Brinkmann, F. Nesch, and L. Zuppiroli, Syn. Met. 146, 387 (2004).
- [11] M. Shtein, J. Mapel, J. B. Benziger, and S. R. Forrest, Appl. Phys. Lett. 81, 268 (2002).
- [12] Y. Qui, Y. Hu, G. Dong, L. Wang, J. Xie, and Y. Ma, Appl. Phys. Lett. 83, 1644 (2003).
- [13] O. D. Jurchescu, J. Baas, and T. T. M. Palstra, Appl. Phys. Lett. 87, 052102 (2005).
- [14] E. A. Silinsh and V. Cápek, Organic molecular crystals, interaction, localization and transport phenomena (AIP press, New York, 1994).

- [15] C. R. Newman, C. D. Frisbie, D. A. da Silva Filfo, J.-L. Brédas, P. C. Ewbank, and K. R. Mann, Chem. Mater. 16, 4436 (2004).
- [16] A. Salleo, Mat. Today **10**, 38 (2007).
- [17] Y. Shirota and H. Kageyama, Chem. Rev. **107**, 953 (2007).
- [18] R. G. Endres, C. Y. Fong, L. H. Yang, G. Witte, and C. Wöll, Comp. Mat. Sci. 29, 362 (2004).
- [19] F. Amy, C. Chan, and A. Kahn, Org. Elect. 6, 85 (2005).
- [20] G. A. de Wijs, C. C. Mattheus, R. A. de Groot, and T. T. M. Palstra, Syn. Met. 139, 109 (2003).
- [21] A. Troisi and G. Orlandi, J. Phys. Chem. B **109**, 1849 (2005).
- [22] I. P. M. Bouchoms, W. A. Schoonveld, J. Vrijmoeth, and T. M. Klapwijk, Syn. Met. **104**, 175 (1999).
- [23] R. Ruiz, D. Choudhary, B. Nickel, T. Toccoli, K.-C. Chang, A. C. Mayer, P. Clancy, J. M. Blakely, R. L. Headrick, S. Iannotta, et al., Chem. Mater. 16, 4497 (2004).
- [24] H. Yanagisawa, T. Tamaki, M. Nakamura, and K. Kudo, Thin Solid Films 464-465, 398 (2004).
- [25] G. Horowitz, Adv. Mat. 10, 365 (1998).
- [26] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, J. Appl. Phys. 87, 4456 (2000).
- [27] J. Zaumseil and H. Sirringhaus, Chem. Rev. **107**, 1296 (2007).
- [28] H. Bässler, Phys. Stat. Sol. (b) **175**, 15 (1993).
- [29] D. M. Pai, J. Chem. Phys. **52**, 2285 (1970).
- [30] W. D. Gill, J. Appl. Phys. 43, 5033 (1972).
- [31] P. G. L. Comber and W. E. Spear, Phys. Rev. Lett. 25, 509 (1970).
- [32] W. Warta and N. Karl, Phys. Rev. B **32**, 1172 (1985).
- [33] M. W. Ashcroft and N. D. Mermin, Solid state physics (Saunders college Publishing, Fort Worth, 1976), college ed.

- [34] M. Pope and C. E. Swenberg, *Electronic processes in organic crystals and polymers* (Oxford University Press, New York, 1999), 2nd ed.
- [35] B. Hartenstein, H. Bässler, S. Heun, P. Borsenberger, M. V. der Auweraer, and F. C. D. Schryyer, Chem. Phys. 191, 321 (1995).
- [36] L. Dennany, E. J. O. Reilly, P. C. Innis, G. G. Wallace, and R. J. Forster, Electroc. Acta 53, 4599 (2008).
- [37] N. Karl, J. Marktanner, R. Stehle, and W. Warta, Syn. Met. 41-43, 2473 (1991).
- [38] D. Knipp, R. A. Street, A. Völkel, and J. Ho, J. Appl. Phys. 93, 347 (2003).
- [39] S. F. Nelson, Y. Y. Lin, D. J. Gundlach, and T. N. Jackson, Appl. Phys. Lett. 72, 1854 (1997).
- [40] M. A. Silinsh, Organic molecular crystals, Their electronic states (Springer-Verlag, Berlin Heidelberg, 1980).
- [41] A. Miller and E. Abrahams, Phys. Rev. **120**, 745 (1960).
- [42] L. B. Schein and J. X. Mack, Chem. Phys. Lett. **149**, 109 (1988).
- [43] R. Schmechel, J. Appl. Phys. **93**, 4653 (2003).
- [44] M. Shur and M. Hack, J. Appl. Phys. 55, 3831 (1984).
- [45] D. K. Schroder, Semiconductor material and device characterization (John Wiley and Sons, 2006), 3rd ed.
- [46] M. Mottaghi and G. Horowitz, Org. Elect. 7, 528 (2006).
- [47] G. Horowitz, R. Hajlaoui, D. Fichou, and A. E. Kassmi, J. Appl. Phys. 85, 3202 (1999).
- [48] A. Facchetti, Mat. Today **10**, 28 (2007).
- [49] E. Menard, M. A. Meitl, Y. Sun, J.-U. Park, D. J.-L. Shir, Y.-S. Nam, S. Jeon, and J. A. Rogers, Chem. Rev. 107, 1117 (2007).
- [50] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, IEEE Trans. Elect. Dev. 48, 1060 (2001).
- [51] K. P. Puntambekar, P. V. Pesavento, and D. Frisbie, Appl. Phys. Lett. 83, 5539 (2003).

- [52] T. Muck, V. Wagner, U. Bass, M. Leufgen, J. Geurts, and L. W. Molenkamp, Syn. Met. 146, 317 (2004).
- [53] T. Muck, J. Fritz, and V. Wagner, Appl. Phys. Lett. 86, 232101 (2005).
- [54] T. G. Bäcklund, H. G. O. Sandberg, R. Osterbacka, H. Stubb, T. Mäkelä, and S. Jussila, Syn. Met. 148, 87 (2005).
- [55] D. Tobjörk, N. J. Kaihovirta, T. Mäkelä, F. S. Pettersson, and R. Österbacka, Org. Elect. 9, 931 (2008).
- [56] J. W. Lim and S. J. Yun, Electrochem. Solid-State Lett. 7, F45 (2004).
- [57] J. Tate, J. A. Rogers, C. D. W. Jones, B. Vyas, D. W. Murphy, W. Li, Z. Bao, R. E. Slusher, A. Dodabalapur, and H. E. Katz, Langmuir 16, 6054 (2000).
- [58] M. Na and S.-W. Rhee, Org. Elect. 7, 205 (2006).
- [59] D. Knipp, R. A. Street, B. Krusor, R. B. Apte, and J. Ho, Proceedings of SPIE 4466, 8 (2001).
- [60] X. Peng, G. Horowitz, D. Fichou, and F. Garnier, Appl. Phys. Lett. 57, 2013 (1990).
- [61] H. L. Hsu, W. C. Yang, Y. L. Lee, and T. R. Yewa, Appl. Phys. Lett. 023501, 91 (2007).
- [62] T. Kawase, T. Shimoda, C. Newsomeb, H. Sirringhaus, and R. H. Friend, Thin Solid Films 438, 279 (2003).
- [63] E. P. R. Choudhury, Handbook of microlithography, micromachining, and microfabrication (SPIE - The International Society for Optical Engineering, Washington, 1997).
- [64] K. Seeger, Semiconductor physics, An introduction (Springer, Berlin, 1999), 7th ed.
- [65] M. Koehler and I. Biaggio, Phys. Rev. B **70**, 045314 (2004).
- [66] R. Bourguiga, M. Mahdouani, S. Mansouri, and G. Horowitz, Eur. Phys. J. Appl. Phys. 39, 7 (2007).
- [67] S. M. Sze, *Physics of semiconductor devices* (John Wiley and Sons, New York, 1981), 2nd ed.

- [68] C. D. Dimitrakopoulos and D. J. Mascaro, IBM J. Res. and Dev. 45, 11 (2001).
- [69] J. E. McDermott, M. McDowell, I. G. Hill, J. Hwang, A. Kahn, S. L. Bernasek, and J. Schwartz, J. Phys. Chem. A 111, 12333 (2007).
- [70] K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, A. N. Rashid, and G. Schitter, J. Phys. Chem. A 111, 12333 (2007).
- [71] H. L. Gomesa, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D. M. de Leeuw, T. Muck, J. Geurts, L. W. Molenkamp, and V. Wagner, Appl. Phys. Lett. 84, 3184 (2004).
- [72] T. Umeda, D. Kumaki, and S. Tokito, Org. Elect. 9, 545 (2008).
- [73] S. R. Forrest, Chem. Rev. 97, 1793 (1997).
- [74] M. A. Herman and H. Sitter, Molecular beam epitaxy, Fundamentals and current status (Springer, Germany, 1996), 2nd ed.
- [75] U. Haas, A. Haase, H. Maresch, B. Stadlober, and G. Leising, IEEE Int. Conf. on Polymers and Adhesives p. 1 (2004).
- [76] S. Verlaak, S. Steudel, P. Heremans, D. Janssen, and M. S. Deleuze, Phys. Rev. B 68, 195409 (2003).
- [77] R. Ruiz, B. Nickel, N. Koch, L. C. Feldman, R. F. Haglund, A. Kahn, F. Family, and G. Scoles, Phys. Rev. Lett. 91, 136102 (2003).
- [78] S. Pratontep, F. Nüesch, L. Zuppiroli, and M. Brinkmann, Phys. Rev. B 72, 085211 (2005).
- [79] D. Kumaki, T. Umeda, and S. Tokito, Appl. Phys. Lett. 92, 093309 (2008).
- [80] AFM probe data sheets: Vecco Instruments (2007), MikroMasch (2008), Oliympus (2008).
- [81] E. Meyer, H. J. Hug, and R. Bennewitz, *Scanning probe microscopy: The lab on a tip* (Springer, Germany, 2004).
- [82] CP-II atomic force microscope user's guide, Vecco Instruments (2006).
- [83] V. Palermo, M. Palma, and P. Samor, Adv. Mat. 18, 145 (2006).

- [84] A. S. Killampalli and J. R. Engstrom, Appl. Phys. Lett. 88, 143125 (2006).
- [85] H. Ichikawa, A. Koma, K. Saiki, and T. Shimada, Surf. Sci. 600, L236 (2006).
- [86] J. B. Koo, S. H. Kim, J. H. Lee, C. H. Ku, S. C. Lima, and T. Zyung, Syn. Met. 156, 99 (2006).
- [87] D. R. Knapp, Handbook of analytical derivatization reactions (John Wiley and Sons, New York, 1979).
- [88] P. R. Choudhury, Handbook of microlithography, micromachining and microfabrication (SPIE optical engineering press, Bellingham, Washington, 1997).
- [89] Delta mask homepage; http://www.deltamask.nl/frames.html.
- [90] Microposit S1813 photoresist data sheets, Microposit (2006).
- [91] Http://www.patentstorm.us/patents/6560020/description.html.
- [92] Http://www.vanderbilt.edu/viibre/documents/Zhang_Lift-Off.doc.
- [93] Http://snf.stanford.edu/Process/Lithography/liftoff.html.
- [94] Microposit LOL1000 resist data sheets, Microposit (2006).
- [95] N. Koch, A. Kahn, J. Ghijsen, J. J. Pireaux, J. Schwartz, R. L. Johnson, and A. Elschner, Appl. Rev. Lett. 82, 70 (2003).
- [96] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts* (Clarendon Press, Oxford, 1988), 2nd ed.
- [97] N. Yoneya, M. Noda, N. Hirai, K. Nomoto, M. Wada, and J. Kasahara, Appl. Phys. Lett. 85, 4663 (2004).
- [98] F. Dinelli, M. Murgia, P. Levy, M. Cavallini, F. Biscarini, and D. M. de Leeuw, Phys. Rev. Lett. 92, 116802 (2004).
- [99] M. Kiguchi, M. Nakayama, K. Fujiwara, K. Ueno, T. Shimada, and K. Saiki, Jpn. J. Appl. Phys. 42, L 1408 L 1410 (2003).
- [100] Y. Y. Noh and D. Y. Kim, Solid-State Elect. **51**, 1052 (2007).
- [101] I. Manunza and A. Bonfiglio, Biosens. Bioelectron. 22, 2775 (2007).

- [102] J. Jang, Mater. Today 9, 46 (2006).
- [103] G. S. Ryu, K. B. Choe, and C. K. Song, Thin Solid Films 514, 302 (2006).
- [104] G. Horowitz, Adv. Mat. **12**, 1046 (2000).
- [105] B. Fraboni, A. Matteucci, A. Cavallini, E. Orgiu, and A. Bonfiglio, Appl. Phys. Lett. 89, 222112 (2006).
- [106] S. Cipolloni, L. Mariucci, A. Valletta, D. Simeone, F. D. Angelis, and G. Fortunato, Thin Solid Films 515, 7546 (2007).
- [107] J. H. Park, C. H. Kang, Y. J. Kim, Y. S. Lee, and J. S. Choi, Mater. Sci. Eng. C 24, 27 (2004).
- [108] R. Ruiz, B. Nickel, N. Koch, L. C. Feldman, R. F. Haglund, A. Kahn, and G. Scoles, Phys. Rev. B 67, 125406 (2005).
- [109] C. D. Dimitrakopoulos, A. R. Brown, and A. Pomp, J. Appl. Phys 80, 2501 (1996).
- [110] B. A. L. Barabasi and H. E. Stanley, Fractal Concepts in Surface Growth (Cambridge University Press, Cambridge, 1995).
- [111] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, et al., Appl. Phys. Lett. 80, 1088 (2002).
- [112] S. Pratontep, M. Brinkmann, N. F, and L. Zuppiroli, Phys. Rev. B 69, 165201 (2004).
- [113] B. Stadlober, U. Haas, H. Maresch, and A. Haase, Phys. Rev. B 74, 165302 (2006).
- [114] L. Bürgi, H. Sirringhaus, and R. H. Friend, Appl. Phys. Lett. 80, 2913 (2002).
- [115] J. A. Nichols, D. J. Gundlach, and T. N. Jackson, Appl. Phys. Lett. 83, 2366 (2003).
- [116] H. Sirringhaus, Adv. Mat **17**, 2411 (2005).
- [117] C. R. Kagan, A. Afzali, and T. O. Graham, Appl. Phys. Lett. 86, 193505 (2005).

- [118] M. Kawaharada, M. Ooishi, T. Saito, and E. Hasegawa, Syn. Met. 91, 113 (1997).
- [119] M. Jørgensen, K. Norrman, and F. C. Krebs, Sol. Energy Mater. Sol. Cells 92, 686 (2008).
- [120] H. L. Cheng, W. Y. Chou, C. W. Kuo, F. C. Tang, and Y. W. Wang, Appl. Phys. Lett. 88, 161918 (2006).
- [121] J. E. Northrup and M. L. Chabinyc, Phys. Rev. B 68, 041202 (2003).
- [122] A. Vollmer, O. D. Jurchescu, I. Arfaoui, I. Salzmann, T. T. M. Palstra, P. Rudolf, J. Niemax, J. Pflaum, J. P. Rabe, and N. Koch, Eur. Phys. J. E 17, 339 (2005).
- [123] D. Li, E. J. Borkent, R. Nortrup, H. Moon, H. Katz, and Z. Bao, Appl. Phys. Lett. 86, 042105 (2005).
- [124] K. Seeger, Semiconductor Physics, An Introduction (Springer, Berlin, 1999), 7th ed.
- [125] Z. T. Zhu, J. T. Mason, R. Dieckmann, and G. G. Malliaras, Appl. Phys. Lett. 81, 4643 (2002).
- [126] D. H. Dunlap, P. E. Parris, and V. M. Kenkre, Phys. Rev. Lett. 77, 542 (1996).